

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
2				*****
3	*			
4	*			Zvector E6 instruction tests for VRR-j encoded:
5	*			
6	*			E67D VCSPH - VECTOR CONVERT HFP TO SCALED DECIMAL
7	*			
8	*			James Wekel June 2024
9	*			*****
11				*****
12	*			
13	*			basic instruction tests
14	*			
15	*			*****
16	*			This program tests proper functioning of the z/arch E6 VRR-j vector
17	*			convert HFP to scaled decimal instruction.
18	*			Exceptions are not tested.
19	*			
20	*			PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
21	*			obvious coding errors. None of the tests are thorough. They are
22	*			NOT designed to test all aspects of any of the instructions.
23	*			
24				*****
25	*			
26	*			A cross-check test is performed if the rounding mode is zero,
27	*			and the shifted packed decimal source can be converted to a 64-bit
28	*			fixed value without overflow. The cross-check test converts the
29	*			packed decimal source, uses CEGR, CDGR or CXGR to convert to
30	*			HFP. This result is compared to VCSPH result. An XCHECK test
31	*			error message will be issued if there is a difference.
32	*			
33				*****
34	*			
35	*			*Testcase zvector-e6-19-VCSPH: VECTOR E6 VRR-j VCSPH instruction
36	*			
37	*			Zvector E6 instruction tests for VRR-j encoded:
38	*			
39	*			E67D VCSPH - VECTOR CONVERT HFP TO SCALED DECIMAL
40	*			
41	*			# -----
42	*			# This tests only the basic function of the instruction.
43	*			# Exceptions are NOT tested.
44	*			# -----
45	*			
46	*	main size	2	
47	*	numcpu	1	
48	*	sysclear		
49	*	archlvl	z/Arch	
50	*			
51	*	loadcore	"\$(testpath)/zvector-e6-19-VCSPH.core"	0x0
52	*			
53	*	diag8cmd	enable	# (needed for messages to Hercules console)
54	*	runtest	2	
55	*	diag8cmd	disable	# (reset back to default)
56	*			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				57 * *Done
				58 *
				59 *****

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
61				*****
62	*			FCHECK Macro - Is a Facility Bit set?
63	*			
64	*			If the facility bit is NOT set, an message is issued and
65	*			the test is skipped.
66	*			
67	*			Fcheck uses R0, R1 and R2
68	*			
69	* eg.			FCHECK 134, 'vector-packed-decimal'
70				*****
71				MACRO
72				FCHECK &BITNO, &NOTSETMSG
73	. *			&BITNO : facility bit number to check
74	. *			&NOTSETMSG : 'facility name'
75	LCLA	&FBBYTE		Facility bit in Byte
76	LCLA	&FBBIT		Facility bit within Byte
77				
78	LCLA	&L(8)		
79	&L(1)	SetA	128, 64, 32, 16, 8, 4, 2, 1	bit positions within byte
80				
81	&FBBYTE	SETA	&BITNO/8	
82	&FBBIT	SETA	&L((&BITNO-(&FBBYTE*8))+1)	
83	. *	MNOTE	0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'	
84				
85	B	X&SYSNDX		
86	*			Fcheck data area
87	*			skip message
88	SKT&SYSNDX	DC	C'	Skipping tests:
89		DC	C&NOTSETMSG	
90		DC	C' facility	(bit &BITNO) is not installed.'
91	SKL&SYSNDX	EQU	*- SKT&SYSNDX	
92	*			facility bits
93	DS	FD		gap
94	FB&SYSNDX	DS	4FD	
95	DS	FD		gap
96	*			
97	X&SYSNDX	EQU	*	
98	LA	R0, ((X&SYSNDX- FB&SYSNDX)/8)-1		
99	STFLE	FB&SYSNDX		get facility bits
100				
101	XGR	R0, R0		
102	IC	R0, FB&SYSNDX+&FBBYTE		get fbit byte
103	N	R0, =F' &FBBIT'		is bit set?
104	BNZ	XC&SYSNDX		
105	*			
106	*	facility bit not set, issue message and exit		
107	*			
108	LA	R0, SKL&SYSNDX		message length
109	LA	R1, SKT&SYSNDX		message address
110	BAL	R2, MSG		
111				
112	B	EOJ		
113	XC&SYSNDX	EQU	*	
114		MEND		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				116 ****	*****	*****
				117 *	Low core PSWs	
				118 ****	*****	*****
00000000	00000000 00000000	0000228F	120 ZVE6TST	START 0 USING ZVE6TST, R0	Low core addressability	
			121			
			122			
	00000140	00000000	123 SVOLDPSW EQU	ZVE6TST+X' 140'	z/Arch Supervisor call old PSW	
00000000	00000000 000001A0	00000000 000001A0	125	ORG ZVE6TST+X' 1A0'	z/Architecture RESTART PSW	
000001A0	00000001 80000000		126	DC X' 0000000180000000'		
000001A8	00000000 00000200		127	DC AD(BEGIN)		
000001B0	000001B0 000001D0	000001B0 000001D0	129	ORG ZVE6TST+X' 1D0'	z/Architecture PROGRAM CHECK PSW	
000001D0	00020001 80000000		130	DC X' 0002000180000000'		
000001D8	00000000 0000DEAD		131	DC AD(X' DEAD')		
000001E0	000001E0 00000200	133	ORG ZVE6TST+X' 200'	Start of actual test program..		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				135 136 ****= 137 * The actual "ZVE6TST" program itself... 138 ****= 139 *
				140 * Architecture Mode: z/Arch 141 * Register Usage: 142 *
				143 * R0 (work) 144 * R1-4 (work) 145 * R5 Testing control table - current test base 146 * R6-R7 (work) 147 * R8 First base register 148 * R9 Second base register 149 * R10 Third base register 150 * R11 E6TEST call return 151 * R12 E6TESTS register 152 * R13 (work) 153 * R14 Subroutine call 154 * R15 Secondary Subroutine call or work 155 * 156 ****=
00000200		00000200		158 USING BEGIN, R8 FIRST Base Register
00000200		00001200		159 USING BEGIN+4096, R9 SECOND Base Register
00000200		00002200		160 USING BEGIN+8192, R10 THIRD Base Register
00000200	0580			161 162 BEGIN BALR R8, 0 Initialize FIRST base register 163 BCTR R8, 0 Initialize FIRST base register 164 BCTR R8, 0 Initialize FIRST base register
00000202	0680			165 166 LA R9, 2048(, R8) Initialize SECOND base register 167 LA R9, 2048(, R9) Initialize SECOND base register
00000204	0680			168 169 LA R10, 2048(, R9) Initialize THIRD base register 170 LA R10, 2048(, R10) Initialize THIRD base register
00000206	4190 8800	00000800		171 172 STCTL R0, R0, CTLR0 Store CRO to enable AFP
0000020A	4190 9800	00000800		173 OI CTLR0+1, X'04' Turn on AFP bit
0000020E	41A0 9800	00000800		174 OI CTLR0+1, X'02' Turn on Vector bit
00000212	41A0 A800	00000800		175 LCTL R0, R0, CTLR0 Reload updated CRO
00000216	B600 83CC	000005CC		176 177 ****= 178 * Is Vector-packed-decimal-enhancement facility 2 installed (bit 192) 179 ****=
0000021A	9604 83CD	000005CD		180 181 FCHECK 192, 'vector-packed-decimal-enhancement facility 2'
0000021E	9602 83CD	000005CD		182+ B X0001 Fcheck data area 183+* skip message
00000222	B700 83CC	000005CC		184+* 185+SKT0001 DC C' Skipping tests: 186+ DC C' vector-packed-decimal-enhancement facility 2' 187+ DC C' facility (bit 192) is not installed.'
00000226	47F0 80C8	000002C8		188+SKL0001 EQU *-SKT0001 189+* 190+ DS FD facility bits gap
0000022A	40404040 40404040			
00000244	A58583A3 96996097			
00000270	40868183 899389A3	0000006B	00000001	
00000298	00000000 00000000			

LOC	OBJECT CODE	ADDR1	ADDR2	STM			
000002A0	00000000 00000000			191+FB0001 192+	DS DS	4FD FD	
000002C0	00000000 00000000			193+*		gap	
000002C8	4100 0004	000002C8	00000001 00000004	194+X0001 195+	EQU LA	*	
000002CC	B2B0 80A0		000002A0	196+	STFLE	RO, ((X0001-FB0001)/8)-1	get facility bits
000002D0	B982 0000			197+	XGR	RO, RO	
000002D4	4300 80B8		000002B8	198+	IC	RO, FB0001+24	get fbit byte
000002D8	5400 83D4		000005D4	199+	N	RO, =F'128'	is bit set?
000002DC	4770 80F0		000002F0	200+ 201+*	BNZ	XC0001	
				202+*	facility bit not set, issue message and exit		
000002E0	4100 006B		0000006B	204+	LA	RO, SKL0001	message length
000002E4	4110 802A		0000022A	205+	LA	R1, SKT0001	message address
000002E8	4520 82E8		000004E8	206+	BAL	R2, MSG	
000002EC	47F0 83B0		000005B0	207+	B	EOJ	
		000002F0	00000001	208+XC0001 209	EQU	*	

LOC	OBJECT CODE	ADDR1	ADDR2	STM			
				211 **** 212 * Do tests in the E6TESTS table 213 ****			
000002F0	58C0 83D8		000005D8	215 L R12, =A(E6TESTS)		get table of test addresses	
000002F4	5850 C000	000002F4	00000001	216 NEXTE6 EQU *			
000002F8	1255		00000000	217 L EQU R5, 0(0, R12)		get test address	
000002FA	4780 82A0		000004A0	218 LTR R5, R5		have a test?	
				219 BZ ENDTEST		done?	
000002FE		00000000		220 221	USING E6TEST, R5		
000002FE	4800 5004		00000004	222 223	LH R0, TNUM	save current test number	
00000302	5000 8E04		00001004	224 225	ST R0, TESTING	for easy reference	
00000306	58B0 5000		00000000	226 227	L R11, TSUB	get address of test routine	
0000030A	05BB			228 229	BALR R11, R11	do test	
0000030C	E710 8EF4 000E		000010F4	230 231	VST V1, V10UTPUT	save result	
00000312	45F0 812E		0000032E	232 233	BAL R15, XCHECK		
00000316	E310 501C 0014		0000001C	234	LGF R1, READDR	expected result address	
0000031C	D50F 8EF4 1000	000010F4	00000000	235	CLC V10UTPUT, 0(R1)		
00000322	4770 8228		00000428	236 237	BNE FAILMSG	no, issue failed message	
00000326	41C0 C004		00000004	238	LA R12, 4(0, R12)	next test address	
0000032A	47F0 80F4		000002F4	239	B NEXTE6		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				241 *-----			
				242 * For small (19 digit) values, cross check result			
				243 * if rounding mode = 0 and conversion to 64-bit does not overflow			
				244 *			
				245 * R15 - RETURN			
				246 *			
				247 * v1, v2, v3 have result, source, scale			
				248 *-----			
0000032E	B982 0011	0000032E	00000001	249 XCHECK	EQU *		
00000332	4310 5008		00000008	250 XGR	R1, R1	Only Xcheck when shift=0	
00000336	1211			251 IC	R1, SCALE	get scale	
00000338	477F 0000		00000000	252 LTR	R1, R1		
				253 BNZ	O(R15)	a scale/shit, so exit	
				254 *			
				255 * convert source extended float to fixed (R0)			
				256 *			
0000033C	E720 8210 000E		00000410	257 VST	V2, XCV2	copy source	
00000342	6840 8210		00000410	258 LD	FPR4, XCV2	load extended HFP	
00000346	6860 8218		00000418	259 LD	FPR6, XCV2+8		
				260			
0000034A	B982 0011			261 XGR	R1, R1	Is Rounding Mode = 0?	
0000034E	4310 5007		00000007	262 IC	R1, M4	get M4	
00000352	A517 0001			263 NILL	r1, 1	RM : bit 3	
00000356	1211			264 LTR	R1, R1		
00000358	4770 8166		00000366	265 BNE	XCR01		
				266 *		no rounding (to 0)	
0000035C	B3CA 0004			267 CGXR	R0, 0, FPR4		
00000360	071F			268 BCR	1, 15	cc=3: overflow: ignore and return	
00000362	47F0 816C		0000036C	269 B	XCR02		
				270 *		Round to nearest with ties away from 0	
00000366	B3CA 1004			271 XCR01	DS OH		
00000366	071F			272 CGXR	R0, 1, FPR4		
				273 BCR	1, 15	cc=3: overflow: ignore and return	
				274 *			
				275 *	result to fixed (R1)		
				276 *			
0000036C	E611 0018 0052			277 XCR02	DS OH		
0000036C	071F			278 VCVBG	R1, V1, 1, 8		
00000372	B9E9 1020			279 BCR	1, 15	cc=3: overflow: ignore and return	
				280 *			
				281 *	values match?		
				282 *			
00000374	4820 5004			283 SGRK	R2, R0, R1	check difference	
00000380	4E20 8ED3		00000004	284 BZ	O(R15)	0k, exit	
00000384	D211 8EBD 8EA7	000010BD	000010D3	285			
0000038A	DE11 8EBD 8ED3	000010BD	000010A7	286 * xcheck failed message			
00000390	D202 8E61 8ECA	00001061	000010D3	287			
00000396	D207 8E83 5010	00001083	00000010	288 LH	R2, TNUM	get test number and convert	
0000039C	B982 0022			289 CVD	R2, DECNUM		
				290 MVC	PRT3, EDIT		
				291 ED	PRT3, DECNUM		
				292 MVC	XCPTNUM(3), PRT3+13	fill in message with test #	
				293			
				294 MVC	XCPNAME, OPNAME	fill in message with instruction	
				295			
				296 XGR	R2, R2	get m4 as U8	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000003A0	4320 5007		00000007	297	IC	R2, M4		
000003A4	4E20 8ED3		000010D3	298	CVD	R2, DECNUM	and convert	
000003A8	D211 8EBD 8EA7	000010BD	000010A7	299	MVC	PRT3, EDIT		
000003AE	DE11 8EBD 8ED3	000010BD	000010D3	300	ED	PRT3, DECNUM		
000003B4	D201 8E94 8ECB	00001094	000010CB	301	MVC	XCPM4(2), PRT3+14	fill in message with m4 field	
				302				
000003BA	B982 0022			303	XGR	R2, R2	get scale as U8	
000003BE	4320 5008		00000008	304	IC	R2, SCALE	and convert	
000003C2	4E20 8ED3		000010D3	305	CVD	R2, DECNUM		
000003C6	D211 8EBD 8EA7	000010BD	000010A7	306	MVC	PRT3, EDIT		
000003CC	DE11 8EBD 8ED3	000010BD	000010D3	307	ED	PRT3, DECNUM		
000003D2	D202 8EA3 8ECA	000010A3	000010CA	308	MVC	XCPSCALE(3), PRT3+13	fill in message with scale field	
				309				
000003D8	50F0 8220		00000420	310	ST	R15, XCR15	save r15	
000003DC	4100 0053		00000053	311	LA	R0, XCPLNG	message length	
000003E0	4110 8E54		00001054	312	LA	R1, XCPLINE	messagfe address	
000003E4	45F0 82AE		000004AE	313	BAL	R15, RPERROR		
				314				
000003E8	58F0 8220		00000420	315	L	R15, XCR15		
000003EC	07FF			316	BR	R15	return from xcheck	
				317				
000003F0				318	DS	OFD		
000003F0	00000000 00000000			319	XCRESLT	DS	XL16	
00000400	00000000 00000000			320	XCV1	DS	XL16	
00000410	00000000 00000000			321	XCV2	DS	XL16	
00000420	00000000 00000000			322	XCR15	DS	FD	
				323				

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				325 ****	*****	*****	*****
				326 * result not as expected:	*****	*****	*****
				327 * issue message with test number, instruction under test	*****	*****	*****
				328 * and instruction m4	*****	*****	*****
				329 *****	*****	*****	*****
00000428	4820 5004	00000428	00000001	330 FAILMSG EQU *	LH R2, TNUM	get test number and convert	
0000042C	4E20 8ED3		00000004	331 CVD R2, DECNUM			
00000430	D211 8EBD 8EA7	000010BD	000010A7	332 MVC PRT3, EDIT			
00000436	DE11 8EBD 8ED3	000010BD	000010D3	334 ED PRT3, DECNUM			
0000043C	D202 8E15 8ECA	00001015	000010CA	335 MVC PRTNUM(3), PRT3+13	PRTNAME, OPNAME	fill in message with test #	
00000442	D207 8E30 5010	00001030	00000010	336			
				337 MVC	PRTNAME, OPNAME	fill in message with instruction	
				338 *			
00000448	B982 0022			339 XGR R2, R2			
0000044C	4320 5007		00000007	340 IC R2, M4	CVD R2, DECNUM	get m4 and convert	
00000450	4E20 8ED3		000010D3	341 MVC PRT3, EDIT			
00000454	D211 8EBD 8EA7	000010BD	000010A7	342 ED PRT3, DECNUM			
0000045A	DE11 8EBD 8ED3	000010BD	000010D3	343 MVC PRTM4(2), PRT3+14	PRTSCALE(3), PRT3+13	fill in message with m4 field	
00000460	D201 8E41 8ECB	00001041	000010CB	344			
				345 *			
00000466	B982 0022			346 XGR R2, R2			
0000046A	4320 5008		00000008	347 IC R2, SCALE	CVD R2, DECNUM	get scale and convert	
0000046E	4E20 8ED3		000010D3	348 MVC PRT3, EDIT			
00000472	D211 8EBD 8EA7	000010BD	000010A7	349 ED PRT3, DECNUM			
00000478	DE11 8EBD 8ED3	000010BD	000010D3	350 MVC PRTSCALE(3), PRT3+13	PRTLINE R12, 4(0, R12)	fill in message with scale	
0000047E	D202 8E50 8ECA	00001050	000010CA	351			
				352 BAL R15, RPERROR			
00000484	4100 004C		0000004C	353 LA R0, PRTLNG	message length		
00000488	4110 8E08		00001008	354 LA R1, PRTLINE	R0, =F' 1'	message address	
0000048C	45F0 82AE		000004AE	355 BAL R15, RPERROR	ST RO, FAILED		
				356			
00000490	5800 83DC	00000490	00000001	357 FAILCONT EQU *			
00000494	5000 8E00		000005DC	360 L R0, =F' 1'	set failed test indicator		
			00001000	361 ST RO, FAILED			
00000498	41C0 C004		00000004	362			
0000049C	47F0 80F4		000002F4	363 LA R12, 4(0, R12)	NEXTE6	next test address	
				364 B			
000004A0	5810 8E00	000004A0	00000001	365 ENDTEST EQU *			
000004A4	1211		00001000	370 L R1, FAILED	did a test fail?		
000004A6	4780 83B0		000005B0	371 LTR R1, R1			
000004AA	47F0 83C8		000005C8	372 BZ EOJ	No, exit		
				373 B FAILTEST	Yes, exit with BAD PSW		
				374			
				375			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				377 ****	*****	*****
				378 * RPTERROR	Report instruction test in error	
				379 *	R0 = MESSGAE LENGTH	
				380 *	R1 = ADDRESS OF MESSAGE	
				381 ****	*****	*****
000004AE	50F0 82CC	000004CC	383	RPTERROR ST	R15, RPTSAVE	Save return address
000004B2	5050 82D0	000004D0	384	ST	R5, RPTSVR5	Save R5
			385 *			
			386 *	Use Hercules Diagnose for Message to console		
			387 *			
000004B6	9002 82D8	000004D8	388	STM	R0, R2, RPTDWSAV	save regs used by MSG
000004BA	4520 82E8	000004E8	389	BAL	R2, MSG	call Hercules console MSG display
000004BE	9802 82D8	000004D8	390	LM	R0, R2, RPTDWSAV	restore regs
000004C2	5850 82D0	000004D0	392	L	R5, RPTSVR5	Restore R5
000004C6	58F0 82CC	000004CC	393	L	R15, RPTSAVE	Restore return address
000004CA	07FF		394	BR	R15	Return to caller
000004CC	00000000		396	RPTSAVE DC	F' 0'	R15 save area
000004D0	00000000		397	RPTSVR5 DC	F' 0'	R5 save area
000004D8	00000000 00000000		399	RPTDWSAV DC	2D' 0'	R0-R2 save area for MSG call

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				401 **** 402 * Issue HERCULES MESSAGE pointed to by R1, length in R0 403 * R2 = return address 404 ****			
000004E8	4900 83E0		000005E0	406 MSG CH R0, =H' 0' 407 BNHR R2		Do we even HAVE a message? No, ignore	
000004EC	07D2						
000004EE	9002 8324		00000524	409 STM R0, R2, MSGSAVE		Save registers	
000004F2	4900 83E2		000005E2	411 CH R0, =AL2(L' MSGMSG)		Message length within limits?	
000004F6	47D0 82FE		000004FE	412 BNH MSGOK		Yes, continue	
000004FA	4100 005F		0000005F	413 LA R0, L' MSGMSG		No, set to maximum	
000004FE	1820			415 MSGOK LR R2, R0		Copy length to work register	
00000500	0620			416 BCTR R2, 0		Minus-1 for execute	
00000502	4420 8330		00000530	417 EX R2, MSGMVC		Copy message to O/P buffer	
00000506	4120 200A		0000000A	419 LA R2, 1+L' MSGCMD(, R2)		Calculate true command length	
0000050A	4110 8336		00000536	420 LA R1, MSGCMD		Point to true command	
0000050E	83120008			422 DC X' 83', X' 12', X' 0008'		Issue Hercules Diagnose X' 008'	
00000512	4780 831E		0000051E	423 BZ MSGRET		Return if successful	
00000516	1222			424			
00000518	4780 831E		0000051E	425 LTR R2, R2 426 BZ MSGRET 427		Is Diag8 Ry (R2) 0? an error occurred but continue	
0000051C	0000			428 DC H' 0'		CRASH for debugging purposes	
0000051E	9802 8324		00000524	430 MSGRET LM R0, R2, MSGSAVE		Restore registers	
00000522	07F2			431 BR R2		Return to caller	
00000524	00000000 00000000			433 MSGSAVE DC 3F' 0'		Registers save area	
00000530	D200 833F 1000	0000053F	00000000	434 MSGMVC MVC MSGMSG(0), 0(R1)		Executed instruction	
00000536	D4E2C7D5 D6C8405C			436 MSGCMD DC C' MSGNOH * '		*** HERCULES MESSAGE COMMAND ***	
0000053F	40404040 40404040			437 MSGMSG DC CL95' '		The message text to be displayed	
438							

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				440 ****	*****	*****
				441 *	Normal completion or Abnormal termination PSWs	
				442 ****	*****	*****
000005A0	00020001 80000000			444 EOJPSW DC OD' 0' , X' 0002000180000000' , AD(0)		
000005B0	B2B2 83A0	000005A0	446 EOJ LPSWE EOJPSW		Normal completion	
000005B8	00020001 80000000			448 FAILPSW DC OD' 0' , X' 0002000180000000' , AD(X' BAD')		
000005C8	B2B2 83B8	000005B8	450 FAILTEST LPSWE FAILPSW		Abnormal termination	
				452 ****	*****	*****
				453 *	Working Storage	
				454 ****	*****	*****
000005CC	00000000		456 CTLR0 DS F		CR0	
000005D0	00000000		457 DS F			
000005D4			459			
000005D4	00000080		460 LTORG ,		Literals pool	
000005D8	000021D0		461 =F' 128'			
000005DC	00000001		462 =A(E6TESTS)			
000005E0	0000		463 =F' 1'			
000005E2	005F		464 =H' 0'			
			465 =AL2(L' MSGMSG)			
			466			
			467 *	some constants		
			468			
	00000400	00000001	469 K EQU 1024		One KB	
	00001000	00000001	470 PAGE EQU (4*K)		Size of one page	
	00010000	00000001	471 K64 EQU (64*K)		64 KB	
	00100000	00000001	472 MB EQU (K*K)		1 MB	
			473			
	AABBCCDD	00000001	474 REG2PATT EQU X' AABBCCDD'		Polluted Register pattern	
	000000DD	00000001	475 REG2LOW EQU X' DD'		(last byte above)	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				477 *=====
				478 *
				479 * NOTE: start data on an address that is easy to display
				480 * within Hercules
				481 *
				482 *=====
				483
000005E4		000005E4	00001000	484 ORG ZVE6TST+X'1000'
00001000	00000000			485 FAILED DC F'0'
00001004	00000000			486 TESTING DC F'0'
				some test failed? current test #
				488 *****
				489 * TEST failed : result messgae
				490 *****
				491 *
				492 * failed message and associated editting
				493 *
00001008	40404040 4040E385			494 PRTLINE DC C' Test # '
00001015	A7A7A7			495 PRTPNUM DC C' xxx'
00001018	40868189 93858440			496 DC c' failed for instruction '
00001030	A7A7A7A7 A7A7A7A7			497 PRTNAME DC CL8'xxxxxxxx'
00001038	40A689A3 884094F4			498 DC C' with m4='
00001041	A7A7			499 PRTM4 DC C' xx'
00001043	6B40A689 A38840A2			500 DC C' , with scale='
00001050	A7A7A7			501 PRTSCALE DC C' xxx'
00001053	4B	0000004C	00000001	502 DC C' . '
				503 PRTLNG EQU *- PRTLINE
				505 *****
				506 * TEST failed : XCHECK
				507 *****
				508 *
				509 * XCHECK failed message
				510 *
00001054	40404040 4040E385			511 XCPLINE DC C' Test # '
00001061	A7A7A7			512 XCPTNUM DC C' xxx'
00001064	40E7C3C8 C5C3D240			513 DC c' XCHECK failed for instruction '
00001083	A7A7A7A7 A7A7A7A7			514 XCPNAME DC CL8'xxxxxxxx'
0000108B	40A689A3 884094F4			515 DC C' with m4='
00001094	A7A7			516 XCPM4 DC C' xx'
00001096	6B40A689 A38840A2			517 DC C' , with scale='
000010A3	A7A7A7			518 XCPSCALE DC C' xxx'
000010A6	4B	00000053	00000001	519 DC C' . '
				520 XCPLNG EQU *- XCPLINE

LOC	OBJECT	CODE	ADDR1	ADDR2	STMT
					522 ****= 523 * TEST failed : message working storage 524 ****= 525 EDIT DC XL18' 402120' 526 527 DC C' ==>' 528 PRT3 DC CL18' ' 529 DC C' <==' 530 DECNUM DS CL16
000010A7	40212020	20202020			
000010B9	7E7E7E6E				
000010BD	40404040	40404040			
000010CF	4C7E7E7E				
000010D3	00000000	00000000			
					532 * 533 * Vector instruction results, pollution and input 534 * 535 DC C' V1 Output ==>' 536 DS OF 537 V1OUTPUT DS XL16 V1 OUTPUT 538 DS XL16 gap 539 V1FUDGE DC XL16' FFFFFFFFFFFFFFFFFFFFFFFFF' 540 V1INPUT DC XL16' 1234567890123456789012345678901D' V1 FUDGE 541 DS XL16 V1 input
000010E3	E5F140D6	A4A397A4			
000010F4	00000000	00000000			
00001104	00000000	00000000			
00001114	FFFFFFFFFF	FFFFFFFFFF			
00001124	12345678	90123456			
00001134	00000000	00000000			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				543 **** 544 * E6TEST DSECT 545 ****
00000000	00000000			547 E6TEST DSECT , 548 TSUB DC A(0), pointer to test
00000004	0000			549 TNUM DC H'00' Test Number
00000006	00			550 DC X'00'
00000007	00			551 M4 DC HL1'00' m4 used
00000008	00			552 SCALE DC HL1'00' scale used
0000000C	00000000			553 V2ADDR DC A(0) address of v2: 16-byte packed decimal
00000010	40404040	40404040		554 OPNAME DC CL8' E6 name
00000018	00000000			555 RELEN DC A(0) result length
0000001C	00000000			556 READDR DC A(0) expected result address
				557 558 ** 559 * test routine will be here (from VRR-j macro)
00001144	00000000	0000228F		561 ZVE6TST CSECT , 562 DS OF
				564 **** 565 * Macros to help build test tables 566 ****
				568 * 569 * macro to generate individual test 570 * 571 MACRO 572 VRR_J &INST, &M4, &SCALE 573 . * &INST - VRR-j instruction under test 574 . * &m4 - m4 field 575 GBLA &TNUM 576 &TNUM SETA &TNUM+1 577 578 DS OFD 579 USING *, R5 base for test data and test routine 580 581 T&TNUM DC A(X&TNUM) address of test routine 582 DC H'&TNUM test number 583 DC X'00' 584 DC HL1'&M4' m4 585 V3_&TNUM DC HL1'&SCALE' scale 586 V2_&TNUM DC A(RE&TNUM+16) address of v2: 16-byte packed decimal 587 DC CL8'&INST' instruction name 588 DC A(16) result length 589 DC A(RE&TNUM) address of expected result 590 . * 591 * 592 X&TNUM DS OF fudge V1 593 VL V1, V1FUDGE

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
594				
595		LGF	R2, V2_&TNUM	get v2
596		VL	V2, 0(R2)	
597				
598		VLEB	V3, V3_&TNUM, 7	get v3 scale
599				
600		&INST	V1, V2, V3, &M4	test instruction
601				
602		BR	R11	return
603				
604	RE&TNUM	DS	OF	expected 16 byte result
605		DROP	R5	
606				
607		MEND		
609	*			
610	*	macro to generate table of pointers to individual tests		
611	*			
612		MACRO		
613		PTTABLE		
614		GBLA	&TNUM	
615		LCLA	&CUR	
616	&CUR	SETA	1	
617	.	*		
618	TTABLE	DS	OF	
619	. LOOP	ANOP		
620	.	*		
621		DC	A(T&CUR)	TEST &CUR
622	.	*		
623	&CUR	SETA	&CUR+1	
624		AIF	(&CUR LE &TNUM). LOOP	
625	*			
626		DC	A(0)	END OF TABLE
627		DC	A(0)	
628	.	*		
629		MEND		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				631 **** 632 * E6 VRR-j tests 633 **** 634 PRINT DATA 635 *
				636 * E67D VCSPH - VECTOR CONVERT HFP TO SCALED DECIMAL 637 * 638 *----- 639 * VCSPH - VECTOR CONVERT HFP TO SCALED DECIMAL 640 *----- 641 * VRR-j instruction, m4, scale(0-31) 642 * followed by 643 * followed by 644 * v1 - 16 byte expected result 645 * v2 - 16 byte extended HFP 646 *----- 647 * No Round - NO Shift 648 *----- 649 * +0 650 VRR_J VCSPH, 0, 0
00001148				651+ DS OFD
00001148		00001148		652+ USING *, R5 base for test data and test routine
00001148	00001168			653+T1 DC A(X1) address of test routine
0000114C	0001			654+ DC H' 1'
0000114E	00			655+ DC X' 00'
0000114F	00			656+ DC HL1' 0'
00001150	00			657+V3_1 DC HL1' 0'
00001154	00001198			658+V2_1 DC A(RE1+16) m4
00001158	E5C3E2D7 C8404040			659+ DC CL8' VCSPH' scale
00001160	00000010			660+ DC A(16) address of v2: 16-byte packed decimal
00001164	00001188			661+ DC A(RE1) instruction name
				662+* result length
00001168				663+X1 DS OF
00001168	E710 8F14 0006	00001114		664+ VL V1, V1FUDGE fudge V1
0000116E	E320 500C 0014	00001154		665+ LGF R2, V2_1 get v2
00001174	E722 0000 0006	00000000		666+ VL V2, 0(R2)
0000117A	E730 5008 7000	00001150		667+ VLEB V3, V3_1, 7 get v3 scale
00001180	E612 3000 007D			668+ VCSPH V1, V2, V3, 0 test instruction
00001186	07FB			669+ BR R11 return
00001188				670+RE1 DS OF expected 16 byte result
00001188				671+ DROP R5
00001188	00000000 00000000			672 DC XL16' 00000000000000000000000000000000C'
00001190	00000000 0000000C			00001198 00000000 00000000
00001198	00000000 00000000			673 DC XL16' 00000000000000000000000000000000'
000011A0	00000000 00000000			000011A8 00000000 00000000
				674 675 * +1
				676 VRR_J VCSPH, 0, 0
000011A8				677+ DS OFD
000011A8		000011A8		678+ USING *, R5 base for test data and test routine
000011A8	000011C8			679+T2 DC A(X2) address of test routine
000011AC	0002			680+ DC H' 2'
000011AE	00			681+ DC X' 00'
000011AF	00			682+ DC HL1' 0'
000011B0	00			683+V3_2 DC HL1' 0'
000011B4	000011F8			684+V2_2 DC A(RE2+16) scale
				address of v2: 16-byte packed decimal

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000011B8	E5C3E2D7 C8404040			685+ DC CL8' VCSPH'		instruction name	
000011C0	00000010			686+ DC A(16)		result length	
000011C4	000011E8			687+ DC A(RE2)		address of expected result	
000011C8				688+* 689+X2 DS OF			
000011C8	E710 8F14 0006	00001114	690+	VL V1, V1FUDGE		fudge V1	
000011CE	E320 500C 0014	000011B4	691+	LGF R2, V2_2		get v2	
000011D4	E722 0000 0006	00000000	692+	VL V2, 0(R2)			
000011DA	E730 5008 7000	000011B0	693+	VLEB V3, V3_2, 7		get v3 scale	
000011E0	E612 3000 007D		694+	VCSPH V1, V2, V3, 0		test instruction	
000011E6	07FB		695+	BR R11		return	
000011E8			696+RE2	DS OF		expected 16 byte result	
000011E8			697+	DROP R5			
000011E8	00000000 00000000		698	DC XL16' 000000000000000000000000000000001C'			
000011F0	00000000 0000001C						
000011F8	41100000 00000000		699	DC XL16' 4110000000000000330000000000000000000000'			
00001200	33000000 00000000						
00001208				700			
00001208				701 * - 1			
00001208	00001228	00001208		702 VRR_J VCSPH, 0, 0			
00001208				703+ DS OFD			
00001208				704+ USING *, R5		base for test data and test routine	
00001208				705+T3 DC A(X3)		address of test routine	
0000120C	0003			706+ DC H' 3'		test number	
0000120E	00			707+ DC X' 00'			
0000120F	00			708+ DC HL1' 0'		m4	
00001210	00			709+V3_3 DC HL1' 0'		scale	
00001214	00001258			710+V2_3 DC A(RE3+16)		address of v2: 16-byte packed decimal	
00001218	E5C3E2D7 C8404040		711+	DC CL8' VCSPH'		instruction name	
00001220	00000010		712+	DC A(16)		result length	
00001224	00001248		713+	DC A(RE3)		address of expected result	
00001224			714+*				
00001228				715+X3 DS OF			
00001228	E710 8F14 0006	00001114	716+	VL V1, V1FUDGE		fudge V1	
0000122E	E320 500C 0014	00001214	717+	LGF R2, V2_3		get v2	
00001234	E722 0000 0006	00000000	718+	VL V2, 0(R2)			
0000123A	E730 5008 7000	00001210	719+	VLEB V3, V3_3, 7		get v3 scale	
00001240	E612 3000 007D		720+	VCSPH V1, V2, V3, 0		test instruction	
00001246	07FB		721+	BR R11		return	
00001248			722+RE3	DS OF		expected 16 byte result	
00001248			723+	DROP R5			
00001248	00000000 00000000		724	DC XL16' 000000000000000000000000000000001D'			
00001250	00000000 0000001D						
00001258	C1100000 00000000		725	DC XL16' C110000000000000B3000000000000000'			
00001260	B3000000 00000000						
00001268				726			
00001268				727 * +9000000000000001 VRR_J VCSPH, 0, 0			
00001268	00001288	00001268	728	DS OFD			
00001268			729+	USING *, R5		base for test data and test routine	
00001268			730+				
0000126C	0004			731+T4 DC A(X4)		address of test routine	
0000126E	00			732+ DC H' 4'		test number	
0000126F	00			733+ DC X' 00'		m4	
00001270	00			734+ DC HL1' 0'		scale	
00001274	000012B8			735+V3_4 DC HL1' 0'		address of v2: 16-byte packed decimal	
00001274				736+V2_4 DC A(RE4+16)			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001278	E5C3E2D7 C8404040			737+ DC CL8' VCSPH'		instruction name	
00001280	00000010			738+ DC A(16)		result length	
00001284	000012A8			739+ DC A(RE4)		address of expected result	
00001288				740+* 741+X4 DS OF			
00001288	E710 8F14 0006	00001114	742+	VL V1, V1FUDGE	fudge V1		
0000128E	E320 500C 0014	00001274	743+	LGF R2, V2_4	get v2		
00001294	E722 0000 0006	00000000	744+	VL V2, 0(R2)			
0000129A	E730 5008 7000	00001270	745+	VLEB V3, V3_4, 7	get v3 scale		
000012A0	E612 3000 007D		746+	VCSPH V1, V2, V3, 0	test instruction		
000012A6	07FB		747+	BR R11	return		
000012A8			748+RE4 DS OF		expected 16 byte result		
000012A8			749+ DROP R5				
000012A8	00000000 00000009		750 DC	XL16' 00000000000000009000000000000001C'			
000012B0	00000000 0000001C						
000012B8	4E1FF973 CAFA8001		751 DC	XL16' 4E1FF973CAFA800140000000000000000'			
000012C0	40000000 00000000						
000012C8				752			
000012C8				753			
000012C8	000012E8	000012C8		754 * - 9223372036854775808			
000012C8	0005			755 VRR_J VCSPH, 0, 0			
000012CE	00			756+ DS OFD			
000012CF	00			757+ USING *, R5	base for test data and test routine		
000012D0	00			758+T5 DC A(X5)	address of test routine		
000012D4	00001318			759+ DC H' 5'	test number		
000012D8	E5C3E2D7 C8404040			760+ DC X' 00'			
000012E0	00000010			761+ DC HL1' 0'	m4		
000012E4	00001308			762+V3_5 DC HL1' 0'	scale		
000012E8				763+V2_5 DC A(RE5+16)	address of v2: 16-byte packed decimal		
000012E8	E710 8F14 0006	00001114	764+ DC CL8' VCSPH'		instruction name		
000012EE	E320 500C 0014	000012D4	765+ DC A(16)		result length		
000012F4	E722 0000 0006	00000000	766+ DC A(RE5)		address of expected result		
000012FA	E730 5008 7000	000012D0	767+*				
00001300	E612 3000 007D		768+X5 DS OF				
00001306	07FB		769+ VL V1, V1FUDGE	fudge V1			
00001308			770+ LGF R2, V2_5	get v2			
00001308	00000000 00009223		771+ VL V2, 0(R2)				
00001310	37203685 4775808D		772+ VLEB V3, V3_5, 7	get v3 scale			
00001318	D0800000 00000000		773+ VCSPH V1, V2, V3, 0	test instruction			
00001320	C2000000 00000000		774+ BR R11	return			
00001320			775+RE5 DS OF	expected 16 byte result			
00001328			776+ DROP R5				
00001328	00001348	00001328	777 DC	XL16' 0000000000009223372036854775808D'			
00001328	0006						
0000132E	00			778 DC XL16' D0800000000000000C2000000000000000'			
0000132F	00			779			
0000132F				780			
0000132F				781 * 9223372036854775807			
0000132F				782 VRR_J VCSPH, 0, 0			
00001328				783+ DS OFD			
00001328				784+ USING *, R5	base for test data and test routine		
00001328	00001348			785+T6 DC A(X6)	address of test routine		
0000132C	0006			786+ DC H' 6'	test number		
0000132E	00			787+ DC X' 00'			
0000132F	00			788+ DC HL1' 0'	m4		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00001330	00			789+V3_6	DC	HL1' 0'
00001334	00001378			790+V2_6	DC	A(RE6+16)
00001338	E5C3E2D7	C8404040		791+	DC	CL8' VCSPH'
00001340	00000010			792+	DC	A(16)
00001344	00001368			793+	DC	A(RE6)
				794+*		
00001348				795+X6	DS	OF
00001348	E710 8F14 0006		00001114	796+	VL	V1, V1FUDGE
0000134E	E320 500C 0014		00001334	797+	LGF	R2, V2_6
00001354	E722 0000 0006		00000000	798+	VL	V2, 0(R2)
0000135A	E730 5008 7000		00001330	799+	VLEB	V3, V3_6, 7
00001360	E612 3000 007D			800+	VCSPH	V1, V2, V3, 0
00001366	07FB			801+	BR	R11
00001368				802+RE6	DS	OF
00001368				803+	DROP	R5
00001368	00000000 00009223			804	DC	XL16' 0000000000009223372036854775807C'
00001370	37203685 4775807C					
00001378	507FFFFF FFFFFFFF			805	DC	XL16' 507FFFFFFFFFFFF42FF000000000000'
00001380	42FF0000 00000000					
				806		
				807		
				808 * 18446744073709551615		
				809	VRR_J	VCSPH, 0, 0
00001388				810+	DS	OFD
00001388		00001388		811+	USING	*, R5
00001388	000013A8			812+T7	DC	A(X7)
0000138C	0007			813+	DC	H' 7'
0000138E	00			814+	DC	X' 00'
0000138F	00			815+	DC	HL1' 0'
00001390	00			816+V3_7	DC	HL1' 0'
00001394	000013D8			817+V2_7	DC	A(RE7+16)
00001398	E5C3E2D7	C8404040		818+	DC	CL8' VCSPH'
000013A0	00000010			819+	DC	A(16)
000013A4	000013C8			820+	DC	A(RE7)
				821+*		
000013A8				822+X7	DS	OF
000013A8	E710 8F14 0006		00001114	823+	VL	V1, V1FUDGE
000013AE	E320 500C 0014		00001394	824+	LGF	R2, V2_7
000013B4	E722 0000 0006		00000000	825+	VL	V2, 0(R2)
000013BA	E730 5008 7000		00001390	826+	VLEB	V3, V3_7, 7
000013C0	E612 3000 007D			827+	VCSPH	V1, V2, V3, 0
000013C6	07FB			828+	BR	R11
000013C8				829+RE7	DS	OF
000013C8				830+	DROP	R5
000013C8	00000000 00018446			831	DC	XL16' 00000000000018446744073709551615C'
000013D0	74407370 9551615C					
000013D8	50FFFFFF FFFFFFFF			832	DC	XL16' 50FFFFFFFFFFFF42FF000000000000'
000013E0	42FF0000 00000000					
				833		
				834 * +1. 25		
000013E8				835	VRR_J	VCSPH, 0, 0
000013E8		000013E8		836+	DS	OFD
000013E8	00001408			837+	USING	*, R5
000013EC	0008			838+T8	DC	A(X8)
000013EE	00			839+	DC	H' 8'
				840+	DC	X' 00'

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000013EF	00			841+	DC	HL1' 0'
000013F0	00			842+V3_8	DC	HL1' 0'
000013F4	00001438			843+V2_8	DC	A(RE8+16)
000013F8	E5C3E2D7 C8404040			844+	DC	CL8' VCSPH'
00001400	00000010			845+	DC	A(16)
00001404	00001428			846+	DC	A(RE8)
				847+*		
00001408				848+X8	DS	OF
00001408	E710 8F14 0006	00001114		849+	VL	V1, V1FUDGE
0000140E	E320 500C 0014	000013F4		850+	LGF	R2, V2_8
00001414	E722 0000 0006	00000000		851+	VL	V2, 0(R2)
0000141A	E730 5008 7000	000013F0		852+	VLEB	V3, V3_8, 7
00001420	E612 3000 007D			853+	VCSPH	V1, V2, V3, 0
00001426	07FB			854+	BR	R11
00001428				855+RE8	DS	OF
00001428				856+	DROP	R5
00001428	00000000 00000000			857	DC	XL16' 000000000000000000000000000000001C'
00001430	00000000 0000001C			858	DC	XL16' 4114000000000000330000000000000000000000'
00001438	41140000 00000000					
00001440	33000000 00000000					
				859		
				860 * +1. 5		
				861	VRR_J	VCSPH, 0, 0
00001448				862+	DS	OFD
00001448		00001448		863+	USING	* , R5
00001448	00001468			864+T9	DC	A(X9)
0000144C	0009			865+	DC	H' 9'
0000144E	00			866+	DC	X' 00'
0000144F	00			867+	DC	HL1' 0'
00001450	00			868+V3_9	DC	HL1' 0'
00001454	00001498			869+V2_9	DC	A(RE9+16)
00001458	E5C3E2D7 C8404040			870+	DC	CL8' VCSPH'
00001460	00000010			871+	DC	A(16)
00001464	00001488			872+	DC	A(RE9)
				873+*		
00001468				874+X9	DS	OF
00001468	E710 8F14 0006	00001114		875+	VL	V1, V1FUDGE
0000146E	E320 500C 0014	00001454		876+	LGF	R2, V2_9
00001474	E722 0000 0006	00000000		877+	VL	V2, 0(R2)
0000147A	E730 5008 7000	00001450		878+	VLEB	V3, V3_9, 7
00001480	E612 3000 007D			879+	VCSPH	V1, V2, V3, 0
00001486	07FB			880+	BR	R11
00001488				881+RE9	DS	OF
00001488				882+	DROP	R5
00001488	00000000 00000000			883	DC	XL16' 000000000000000000000000000000001C'
00001490	00000000 0000001C			884	DC	XL16' 4118000000000000330000000000000000000000'
00001498	41180000 00000000					
000014A0	33000000 00000000					
				885		
				886 * +1. 75		
				887	VRR_J	VCSPH, 0, 0
000014A8				888+	DS	OFD
000014A8		000014A8		889+	USING	* , R5
000014A8	000014C8			890+T10	DC	A(X10)
000014AC	000A			891+	DC	H' 10'
000014AE	00			892+	DC	X' 00'

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000014AF	00			893+ DC HL1' 0'		
000014B0	00			894+V3_10 DC HL1' 0'	m4 scale	
000014B4	000014F8			895+V2_10 DC A(RE10+16)	address of v2: 16-byte packed decimal	
000014B8	E5C3E2D7 C8404040			896+ DC CL8' VCSPH'	instruction name	
000014C0	00000010			897+ DC A(16)	result length	
000014C4	000014E8			898+ DC A(RE10)	address of expected result	
000014C8				899+* 900+X10 DS OF		
000014C8	E710 8F14 0006	00001114	901+	VL V1, V1FUDGE	fudge V1	
000014CE	E320 500C 0014	000014B4	902+	LGF R2, V2_10	get v2	
000014D4	E722 0000 0006	00000000	903+	VL V2, 0(R2)		
000014DA	E730 5008 7000	000014B0	904+	VLEB V3, V3_10, 7	get v3 scale	
000014E0	E612 3000 007D		905+	VCSPH V1, V2, V3, 0	test instruction	
000014E6	07FB		906+	BR R11	return	
000014E8			907+RE10 DS OF		expected 16 byte result	
000014E8			908+ DROP R5			
000014E8	00000000 00000000		909 DC	XL16' 000000000000000000000000000000001C'		
000014F0	00000000 0000001C		910 DC	XL16' 411C000000000000330000000000000000000000'		
000014F8	411C0000 00000000					
00001500	33000000 00000000					
			911 *-			
			912 * NO Round - with shifts			
			913 *-			
			914			
			915 * +0			
00001508			916 VRR_J VCSPH, 0, 1			
00001508		00001508	917+ DS OFD			
00001508	00001528		918+ USING *, R5		base for test data and test routine	
00001508	00001528		919+T11 DC A(X11)		address of test routine	
0000150C	000B		920+ DC H' 11'		test number	
0000150E	00		921+ DC X' 00'			
0000150F	00		922+ DC HL1' 0'		m4	
00001510	01		923+V3_11 DC HL1' 1'		scale	
00001514	00001558		924+V2_11 DC A(RE11+16)		address of v2: 16-byte packed decimal	
00001518	E5C3E2D7 C8404040		925+ DC CL8' VCSPH'		instruction name	
00001520	00000010		926+ DC A(16)		result length	
00001524	00001548		927+ DC A(RE11)		address of expected result	
00001528			928+*			
00001528	E710 8F14 0006	00001114	929+X11 DS OF		fudge V1	
0000152E	E320 500C 0014	00001514	930+ VL V1, V1FUDGE		get v2	
00001534	E722 0000 0006	00000000	931+ LGF R2, V2_11			
0000153A	E730 5008 7000	00001510	932+ VL V2, 0(R2)			
00001540	E612 3000 007D		933+ VLEB V3, V3_11, 7		get v3 scale	
00001546	07FB		934+ VCSPH V1, V2, V3, 0		test instruction	
00001548			935+ BR R11		return	
00001548			936+RE11 DS OF		expected 16 byte result	
00001548	00000000 00000000		937+ DROP R5			
00001548	00000000 0000000C		938 DC	XL16' 00000000000000000000000000000000C'		
00001550	00000000 00000000		939 DC	XL16' 00000000000000000000000000000000'		
00001558	00000000 00000000					
00001560	00000000 00000000					
			940			
			941 * +1			
00001568		00001568	942 VRR_J VCSPH, 0, 1			
00001568		00001568	943+ DS OFD			
			944+ USING *, R5		base for test data and test routine	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000016E8				1049 1050+	VRR_J VCSPH, 0, 2 DS OFD	
000016E8		000016E8		1051+ 1052+T16 1053+	USING *, R5 DC A(X16) DC H' 16'	base for test data and test routine address of test routine test number
000016EC	0010			1054+ 1055+ 1056+V3_16	DC X' 00' DC HL1' 0' DC HL1' 2'	m4 scale
000016EE	00			1057+V2_16	DC A(RE16+16)	address of v2: 16-byte packed decimal
000016EF	00			1058+	DC CL8' VCSPH'	instruction name
000016F0	02			1059+	DC A(16)	result length
000016F4	00001738			1060+ 1061+*	DC A(RE16)	address of expected result
000016F8	E5C3E2D7 C8404040			1062+X16	DS OF	
00001700	00000010			1063+	VL V1, V1FUDGE	fudge V1
00001704	00001728			1064+	LGF R2, V2_16	get v2
00001708	E710 8F14 0006	00001114		1065+	VL V2, 0(R2)	
0000170E	E320 500C 0014	000016F4		1066+	VLEB V3, V3_16, 7	get v3 scale
00001714	E722 0000 0006	00000000		1067+	VCSPH V1, V2, V3, 0	test instruction
0000171A	E730 5008 7000	000016F0		1068+	BR R11	return
00001720	E612 3000 007D			1069+RE16	DS OF	expected 16 byte result
00001726	07FB			1070+	DROP R5	
00001728	00000000 00922337			1071	DC XL16' 0000000000922337203685477580700C'	
00001730	20368547 7580700C			1072	DC XL16' 507FFFFFFFFFFFF42FF000000000000'	
00001738	507FFFFF FFFFFFFF			1073		
00001740	42FF0000 00000000			1074		
				1075 * 18446744073709551615		
00001748				1076	VRR_J VCSPH, 0, 2	
00001748		00001748		1077+	DS OFD	
00001748	00001768			1078+	USING *, R5	base for test data and test routine
0000174C	0011			1079+T17	DC A(X17)	address of test routine
0000174E	00			1080+	DC H' 17'	test number
0000174F	00			1081+	DC X' 00'	
00001750	02			1082+	DC HL1' 0'	m4
00001754	00001798			1083+V3_17	DC HL1' 2'	scale
00001758	E5C3E2D7 C8404040			1084+V2_17	DC A(RE17+16)	address of v2: 16-byte packed decimal
00001760	00000010			1085+	DC CL8' VCSPH'	instruction name
00001764	00001788			1086+	DC A(16)	result length
00001768	E710 8F14 0006	00001114		1087+	DC A(RE17)	address of expected result
00001768	E320 500C 0014			1088+*		
0000176E	E320 500C 0014	00001754		1089+X17	DS OF	
00001774	E722 0000 0006	00000000		1090+	VL V1, V1FUDGE	fudge V1
0000177A	E730 5008 7000	00001750		1091+	LGF R2, V2_17	get v2
00001780	E612 3000 007D			1092+	VL V2, 0(R2)	
00001786	07FB			1093+	VLEB V3, V3_17, 7	get v3 scale
00001788	00000000 01844674			1094+	VCSPH V1, V2, V3, 0	test instruction
00001788	40737095 5161500C			1095+	BR R11	return
00001790	50FFFFFF FFFFFFFF			1096+RE17	DS OF	expected 16 byte result
00001798	42FF0000 00000000			1097+	DROP R5	
000017A0				1098	DC XL16' 00000000001844674407370955161500C'	
				1099	DC XL16' 50FFFFFF FFFFFFFF42FF000000000000'	
				1100		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
000019D0	00000000 0000001D				
000019D8	C1100000 00000000		1259	DC	XL16' C11000000000000B3000000000000000'
000019E0	B3000000 00000000				
			1260		
			1261		
			1262 * +9000000000000001		
			1263 VRR_J VCSPH, 1, 0		
000019E8		000019E8	1264+ DS OFD		
000019E8	00001A08		1265+ USING *, R5		base for test data and test routine
000019EC	0018		1266+T24 DC A(X24)		address of test routine
000019EE	00		1267+ DC H' 24'		test number
000019EF	01		1268+ DC X' 00'		
000019F0	00		1269+ DC HL1' 1'		m4
000019F4	00001A38		1270+V3_24 DC HL1' 0'		scale
000019F8	E5C3E2D7 C8404040		1271+V2_24 DC A(RE24+16)		address of v2: 16-byte packed decimal
00001A00	00000010		1272+ DC CL8' VCSPH'		instruction name
00001A04	00001A28		1273+ DC A(16)		result length
00001A08			1274+ DC A(RE24)		address of expected result
00001A08	E710 8F14 0006	00001114	1275+* 1276+X24 DS OF		
00001A0E	E320 500C 0014	000019F4	1277+ VL V1, V1FUDGE		fudge V1
00001A14	E722 0000 0006	00000000	1278+ LGF R2, V2_24		get v2
00001A1A	E730 5008 7000	000019F0	1279+ VL V2, 0(R2)		
00001A20	E612 3010 007D		1280+ VLEB V3, V3_24, 7		get v3 scale
00001A26	07FB		1281+ VCSPH V1, V2, V3, 1		test instruction
00001A28			1282+ BR R11		return
00001A28			1283+RE24 DS OF		expected 16 byte result
00001A28			1284+ DROP R5		
00001A28	00000000 00000009		1285 DC XL16' 000000000000000090000000000000001C'		
00001A30	00000000 0000001C				
00001A38	4E1FF973 CAFA8001		1286 DC XL16' 4E1FF973CAFA80014000000000000000'		
00001A40	40000000 00000000				
			1287		
			1288		
			1289 * - 9223372036854775808		
00001A48		00001A48	1290 VRR_J VCSPH, 1, 0		
00001A48	00001A68		1291+ DS OFD		
00001A48	0019		1292+ USING *, R5		base for test data and test routine
00001A4C	00		1293+T25 DC A(X25)		address of test routine
00001A4E	00		1294+ DC H' 25'		test number
00001A4F	01		1295+ DC X' 00'		
00001A50	00		1296+ DC HL1' 1'		m4
00001A54	00001A98		1297+V3_25 DC HL1' 0'		scale
00001A58	E5C3E2D7 C8404040		1298+V2_25 DC A(RE25+16)		address of v2: 16-byte packed decimal
00001A60	00000010		1299+ DC CL8' VCSPH'		instruction name
00001A64	00001A88		1300+ DC A(16)		result length
00001A64			1301+ DC A(RE25)		address of expected result
00001A68			1302+* 1303+X25 DS OF		
00001A68	E710 8F14 0006	00001114	1304+ VL V1, V1FUDGE		fudge V1
00001A6E	E320 500C 0014	00001A54	1305+ LGF R2, V2_25		get v2
00001A74	E722 0000 0006	00000000	1306+ VL V2, 0(R2)		
00001A7A	E730 5008 7000	00001A50	1307+ VLEB V3, V3_25, 7		get v3 scale
00001A80	E612 3010 007D		1308+ VCSPH V1, V2, V3, 1		test instruction
00001A86	07FB		1309+ BR R11		return
00001A88			1310+RE25 DS OF		expected 16 byte result

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00001A88				1311+	DROP	R5
00001A88	00000000 00009223			1312	DC	XL16' 0000000000009223372036854775808D'
00001A90	37203685 4775808D					
00001A98	D0800000 00000000			1313	DC	XL16' D0800000000000000C2000000000000000'
00001AA0	C2000000 00000000					
				1314		
				1315		
				1316 *	9223372036854775807	
00001AA8				1317	VRR_J	VCSPH, 1, 0
00001AA8		00001AA8		1318+	DS	OFD
00001AA8	00001AC8			1319+	USING	* , R5
00001AAC	001A			1320+T26	DC	A(X26)
00001AAE	00			1321+	DC	H' 26'
00001AAF	01			1322+	DC	X' 00'
00001AB0	00			1323+	DC	HL1' 1'
00001AB4	00001AF8			1324+V3_26	DC	HL1' 0'
00001AB8	E5C3E2D7 C8404040			1325+V2_26	DC	A(RE26+16)
00001AC0	00000010			1326+	DC	CL8' VCSPH'
00001AC4	00001AE8			1327+	DC	A(16)
				1328+	DC	A(RE26)
				1329+*		
00001AC8				1330+X26	DS	OF
00001AC8	E710 8F14 0006		00001114	1331+	VL	V1, V1FUDGE
00001ACE	E320 500C 0014		00001AB4	1332+	LGF	R2, V2_26
00001AD4	E722 0000 0006		00000000	1333+	VL	V2, 0(R2)
00001ADA	E730 5008 7000		00001AB0	1334+	VLEB	V3, V3_26, 7
00001AE0	E612 3010 007D			1335+	VCSPH	V1, V2, V3, 1
00001AE6	07FB			1336+	BR	R11
00001AE8				1337+RE26	DS	OF
						expected 16 byte result
00001AE8				1338+	DROP	R5
00001AE8	00000000 00009223			1339	DC	XL16' 0000000000009223372036854775807C'
00001AF0	37203685 4775807C					
00001AF8	507FFFF FFFFFFFF			1340	DC	XL16' 507FFFFFFFFFFFF42FF000000000000'
00001B00	42FF0000 00000000					
				1341		
				1342		
				1343 *	18446744073709551615	
00001B08				1344	VRR_J	VCSPH, 1, 0
00001B08		00001B08		1345+	DS	OFD
00001B08	00001B28			1346+	USING	* , R5
00001B0C	001B			1347+T27	DC	A(X27)
00001BOE	00			1348+	DC	H' 27'
00001BOF	01			1349+	DC	X' 00'
00001B10	00			1350+	DC	HL1' 1'
00001B14	00001B58			1351+V3_27	DC	HL1' 0'
00001B18	E5C3E2D7 C8404040			1352+V2_27	DC	A(RE27+16)
00001B20	00000010			1353+	DC	CL8' VCSPH'
00001B24	00001B48			1354+	DC	A(16)
				1355+	DC	A(RE27)
				1356+*		
00001B28				1357+X27	DS	OF
00001B28	E710 8F14 0006		00001114	1358+	VL	V1, V1FUDGE
00001B2E	E320 500C 0014		00001B14	1359+	LGF	R2, V2_27
00001B34	E722 0000 0006		00000000	1360+	VL	V2, 0(R2)
00001B3A	E730 5008 7000		00001B10	1361+	VLEB	V3, V3_27, 7
00001B40	E612 3010 007D			1362+	VCSPH	V1, V2, V3, 1
						get v3 scale
						test instruction

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001B46	07FB			1363+ 1364+RE27	BR DS	R11 OF	return expected 16 byte result
00001B48				1365+ 1366	DROP DC	R5	
00001B48	00000000 00018446					XL16' 0000000000018446744073709551615C'	
00001B50	74407370 9551615C						
00001B58	50FFFFFF FFFFFFFF			1367	DC	XL16' 50FFFFFFFFFFFF42FF000000000000'	
00001B60	42FF0000 00000000			1368			
				1369			
				1370 * 9009000000018446744073709551615			
				1371		VRR_J VCSPH, 1, 0	
00001B68				1372+	DS	OFD	
00001B68	00001B88	00001B68		1373+ 1374+T28	USING *	, R5	base for test data and test routine
00001B68	001C			1375+	DC	A(X28)	address of test routine
00001B6C	00			1376+	DC	H' 28'	test number
00001B6E	01			1377+	DC	X' 00'	
00001B70	00			1378+V3_28	DC	HL1' 1'	m4
00001B74	00001BB8			1379+V2_28	DC	HL1' 0'	scale
00001B78	E5C3E2D7 C8404040			1380+	DC	A(RE28+16)	address of v2: 16-byte packed decimal
00001B80	00000010			1381+	DC	CL8' VCSPH'	instruction name
00001B84	00001BA8			1382+	DC	A(16)	result length
				1383+*	DC	A(RE28)	address of expected result
00001B88				1384+X28	DS	OF	
00001B88	E710 8F14 0006		00001114	1385+	VL	V1, V1FUDGE	fudge V1
00001B8E	E320 500C 0014		00001B74	1386+	LGF	R2, V2_28	get v2
00001B94	E722 0000 0006		00000000	1387+	VL	V2, 0(R2)	
00001B9A	E730 5008 7000		00001B70	1388+	VLEB	V3, V3_28, 7	get v3 scale
00001BA0	E612 3010 007D			1389+	VCSPH	V1, V2, V3, 1	test instruction
00001BA6	07FB			1390+	BR	R11	return
00001BA8				1391+RE28	DS	OF	expected 16 byte result
00001BA8	90090000 00018446			1392+	DROP	R5	
00001BB0	74407370 9551615C			1393	DC	XL16' 9009000000018446744073709551615C'	
00001BB8	5A71B5A6 23751870			1394	DC	XL16' 5A71B5A6237518704CDF6067FFFFF00'	
00001BC0	4CDF6067 FFFFFF00			1395			
				1396			
				1397 * 999999990018446744073709551615			
00001BC8				1398		VRR_J VCSPH, 1, 0	
00001BC8	00001BE8	00001BC8		1399+ 1400+	DS	OFD	base for test data and test routine
00001BC8	0001BE8			1401+T29	USING *	, R5	address of test routine
00001BCC	001D			1402+	DC	A(X29)	test number
00001BCE	00			1403+	DC	H' 29'	
00001BCF	01			1404+	DC	X' 00'	m4
00001BD0	00			1405+V3_29	DC	HL1' 1'	scale
00001BD4	00001C18			1406+V2_29	DC	HL1' 0'	address of v2: 16-byte packed decimal
00001BD8	E5C3E2D7 C8404040			1407+	DC	A(RE29+16)	instruction name
00001BE0	00000010			1408+	DC	CL8' VCSPH'	result length
00001BE4	00001C08			1409+	DC	A(16)	address of expected result
				1410+*	DC	A(RE29)	
00001BE8				1411+X29	DS	OF	
00001BE8	E710 8F14 0006		00001114	1412+	VL	V1, V1FUDGE	fudge V1
00001BEE	E320 500C 0014		00001BD4	1413+	LGF	R2, V2_29	get v2
00001BF4	E722 0000 0006		00000000	1414+	VL	V2, 0(R2)	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001CBA	E730 5008 7000		00001C90	1467+ 1468+	VLEB VCSPH	V3, V3_31, 7 V1, V2, V3, 1	get v3 scale test instruction
00001CC0	E612 3010 007D			1469+ 1470+RE31 1471+	BR DS DROP	R11 OF R5	return expected 16 byte result
00001CC6	07FB			1472	DC	XL16' 000000000000000000000000000000002C'	
00001CC8	00000000 00000000			1473	DC	XL16' 4118000000000000330000000000000000000000'	
00001CD0	00000000 0000002C			1474 1475 * +1.75			
00001CD8	41180000 00000000			1476	VRR_J	VCSPH, 1, 0	
00001CE0	33000000 00000000			1477+ 1478+	DS USING	OFD *, R5	base for test data and test routine
00001CE8	00001D08	00001CE8		1479+T32	DC	A(X32)	address of test routine
00001CEC	0020			1480+	DC	H' 32'	test number
00001CEE	00			1481+	DC	X' 00'	
00001CEF	01			1482+	DC	HL1' 1'	m4
00001CF0	00			1483+V3_32 1484+V2_32	DC	HL1' 0'	scale
00001CF4	00001D38				DC	A(RE32+16)	address of v2: 16-byte packed decimal
00001CF8	E5C3E2D7 C8404040			1485+	DC	CL8' VCSPH'	instruction name
00001D00	00000010			1486+	DC	A(16)	result length
00001D04	00001D28			1487+	DC	A(RE32)	address of expected result
00001D08				1488+*			
00001D08	E710 8F14 0006	00001114		1489+X32	DS	OF	
00001D0E	E320 500C 0014	00001CF4		1490+	VL	V1, V1FUDGE	fudge V1
00001D14	E722 0000 0006	00000000		1491+	LGF	R2, V2_32	get v2
00001D1A	E730 5008 7000	00001CF0		1492+	VL	V2, 0(R2)	
00001D20	E612 3010 007D		00001114	1493+	VLEB	V3, V3_32, 7	get v3 scale
00001D26	07FB			1494+	VCSPH	V1, V2, V3, 1	test instruction
00001D28				1495+	BR	R11	return
00001D28	00000000 00000000			1496+RE32	DS	OF	expected 16 byte result
00001D28	00000000 0000002C			1497+	DROP	R5	
00001D30	00000000 0000002C			1498	DC	XL16' 000000000000000000000000000000002C'	
00001D38	411C0000 00000000			1499	DC	XL16' 411C000000000000330000000000000000000000'	
00001D40	33000000 00000000			1500			
00001D48				1501 *--			
00001D48	00001D68	00001D48		1502 * ROUND - with shifts			
00001D48	0021			1503 *			
00001D4E	00			1504 * +0			
00001D4F	01			1505	VRR_J	VCSPH, 1, 1	
00001D50	01			1506+	DS	OFD	
00001D54	00001D98			1507+	USING	*, R5	base for test data and test routine
00001D58	E5C3E2D7 C8404040			1508+T33	DC	A(X33)	address of test routine
00001D60	00000010			1509+	DC	H' 33'	test number
00001D64	00001D88			1510+	DC	X' 00'	m4
00001D68				1511+	DC	HL1' 1'	scale
				1512+V3_33	DC	HL1' 1'	
				1513+V2_33	DC	A(RE33+16)	address of v2: 16-byte packed decimal
				1514+	DC	CL8' VCSPH'	instruction name
				1515+	DC	A(16)	result length
				1516+	DC	A(RE33)	address of expected result
				1517+*			
				1518+X33	DS	OF	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001EE4	00001F08			1623+ 1624+*	DC	A(RE37)	address of expected result
00001EE8	E710 8F14 0006		00001114	1625+X37	DS	OF	
00001EEE	E320 500C 0014		00001ED4	1626+ 1627+	VL	V1, V1FUDGE	fudge V1
00001EF4	E722 0000 0006		00000000	1628+	LGF	R2, V2_37	get v2
00001EFA	E730 5008 7000		00001ED0	1629+	VL	V2, 0(R2)	
00001F00	E612 3010 007D			1630+	VLEB	V3, V3_37, 7	get v3 scale
00001F06	07FB			1631+	VCSPH	V1, V2, V3, 1	test instruction
00001F08				1632+RE37	BR	R11	return
00001F08				1633+	DS	OF	expected 16 byte result
00001F08	00000000 00922337			1634	DROP	R5	
00001F10	20368547 7580800D				DC	XL16' 0000000000922337203685477580800D'	
00001F18	D0800000 00000000			1635	DC	XL16' D0800000000000000C2000000000000000'	
00001F20	C2000000 00000000			1636			
				1637			
				1638 * 9223372036854775807			
00001F28		00001F28		1639	DS	VRR_J VCSPH, 1, 2	
00001F28	00001F48			1640+	USING	*, R5	base for test data and test routine
00001F2C	0026			1641+ 1642+T38	DC	A(X38)	address of test routine
00001F2E	00			1643+	DC	H' 38'	test number
00001F2F	01			1644+	DC	X' 00'	
00001F30	02			1645+	DC	HL1' 1'	m4
00001F34	00001F78			1646+V3_38	DC	HL1' 2'	scale
00001F38	E5C3E2D7 C8404040			1647+V2_38	DC	A(RE38+16)	address of v2: 16-byte packed decimal
00001F40	00000010			1648+	DC	CL8' VCSPH'	instruction name
00001F44	00001F68			1649+	DC	A(16)	result length
00001F48				1650+	DC	A(RE38)	address of expected result
00001F48	1651+*			1652+X38	DS	OF	
00001F48	E710 8F14 0006		00001114	1653+	VL	V1, V1FUDGE	fudge V1
00001F4E	E320 500C 0014		00001F34	1654+	LGF	R2, V2_38	get v2
00001F54	E722 0000 0006		00000000	1655+	VL	V2, 0(R2)	
00001F5A	E730 5008 7000		00001F30	1656+	VLEB	V3, V3_38, 7	get v3 scale
00001F60	E612 3010 007D			1657+	VCSPH	V1, V2, V3, 1	test instruction
00001F66	07FB			1658+	BR	R11	return
00001F68				1659+RE38	DS	OF	expected 16 byte result
00001F68				1660+	DROP	R5	
00001F68	00000000 00922337			1661	DC	XL16' 0000000000922337203685477580700C'	
00001F70	20368547 7580700C			1662	DC	XL16' 507FFFFFFFFFFFF42FF0000000000000'	
00001F78	507FFFFF FFFFFFFF			1663			
00001F80	42FF0000 00000000			1664			
				1665 * 18446744073709551615			
00001F88		00001F88		1666	DS	VRR_J VCSPH, 1, 2	
00001F88	00001FA8			1667+	USING	*, R5	base for test data and test routine
00001F88	0027			1668+ 1669+T39	DC	A(X39)	address of test routine
00001F8C	0027			1670+	DC	H' 39'	test number
00001F8E	00			1671+	DC	X' 00'	
00001F8F	01			1672+	DC	HL1' 1'	m4
00001F90	02			1673+V3_39	DC	HL1' 2'	scale
00001F94	00001FD8			1674+V2_39	DC	A(RE39+16)	address of v2: 16-byte packed decimal

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001F98	E5C3E2D7 C8404040			1675+ DC CL8' VCSPH'		instruction name	
00001FA0	00000010			1676+ DC A(16)		result length	
00001FA4	00001FC8			1677+ DC A(RE39)		address of expected result	
00001FA8				1678+* 1679+X39 DS OF			
00001FA8	E710 8F14 0006	00001114	1680+	VL V1, V1FUDGE	fudge V1		
00001FAE	E320 500C 0014	00001F94	1681+	LGF R2, V2_39	get v2		
00001FB4	E722 0000 0006	00000000	1682+	VL V2, 0(R2)			
00001FBA	E730 5008 7000	00001F90	1683+	VLEB V3, V3_39, 7	get v3 scale		
00001FC0	E612 3010 007D		1684+	VCSPH V1, V2, V3, 1	test instruction		
00001FC6	07FB		1685+	BR R11	return		
00001FC8			1686+RE39	DS OF	expected 16 byte result		
00001FC8			1687+	DROP R5			
00001FC8	00000000 01844674		1688	DC XL16' 0000000001844674407370955161500C'			
00001FD0	40737095 5161500C			1689 DC XL16' 50FFFFFF42FF000000000000'			
00001FD8	50FFFFFF FFFFFFFF						
00001FE0	42FF0000 00000000						
			1690				
			1691				
			1692 * 9009000000018446744073709551615				
00001FE8			1693 VRR_J VCSPH, 1, 3				
00001FE8		00001FE8	1694+ DS OFD				
00001FE8	00002008		1695+ USING *, R5		base for test data and test routine		
00001FEC	0028				address of test routine		
00001FEE	00				test number		
00001FEE	01				m4		
00001FF0	03		1696+T40 DC A(X40)		scale		
00001FF4	00002038		1697+ DC H' 40'		address of v2: 16-byte packed decimal		
00001FF8	E5C3E2D7 C8404040		1698+ DC X' 00'				
00002000	00000010	00001114	1699+ DC HL1' 1'				
00002004	00002028		1700+V3_40 DC HL1' 3'				
00002008			1701+V2_40 DC A(RE40+16)				
00002008	E710 8F14 0006		1702+ DC CL8' VCSPH'		instruction name		
0000200E	E320 500C 0014	00001FF4	1703+ DC A(16)		result length		
00002014	E722 0000 0006	00000000	1704+ DC A(RE40)		address of expected result		
0000201A	E730 5008 7000	00001FF0	1705+*				
00002008	07FB		1706+X40 DS OF				
00002020			1707+ VL V1, V1FUDGE	fudge V1			
00002026			1708+ LGF R2, V2_40	get v2			
00002028			1709+ VL V2, 0(R2)				
00002028	90000000 18446744		1710+ VLEB V3, V3_40, 7	get v3 scale			
00002030	07370955 1615000C			VCSPH V1, V2, V3, 1	test instruction		
00002038	5A71B5A6 23751870		1711+ BR R11	return			
00002040	4CDF6067 FFFFFF00		1712+ DS OF	expected 16 byte result			
			1713+RE40 DROP R5				
			1714+ DC XL16' 900000001844674407370955161500C'				
			1715 DC XL16' 5A71B5A6237518704CDF6067FFFFF00'				
			1716 DC				
			1717				
			1718				
			1719 * 9999999990018446744073709551615				
00002048			1720 VRR_J VCSPH, 1, 3				
00002048		00002048	1721+ DS OFD				
00002048	00002068		1722+ USING *, R5		base for test data and test routine		
0000204C	0029		1723+T41 DC A(X41)		address of test routine		
0000204E	00		1724+ DC H' 41'		test number		
0000204F	01		1725+ DC X' 00'		m4		
			1726+ DC HL1' 1'				

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00002050	03			1727+V3_41	DC	HL1' 3'
00002054	00002098			1728+V2_41	DC	A(RE41+16)
00002058	E5C3E2D7	C8404040		1729+	DC	CL8' VCSPH'
00002060	00000010			1730+	DC	A(16)
00002064	00002088			1731+	DC	A(RE41)
				1732+*		scale
00002068				1733+X41	DS	OF
00002068	E710 8F14 0006	00001114		1734+	VL	V1, V1FUDGE
0000206E	E320 500C 0014	00002054		1735+	LGF	R2, V2_41
00002074	E722 0000 0006	00000000		1736+	VL	V2, 0(R2)
0000207A	E730 5008 7000	00002050		1737+	VLEB	V3, V3_41, 7
00002080	E612 3010 007D			1738+	VCSPH	V1, V2, V3, 1
00002086	07FB			1739+	BR	R11
00002088				1740+RE41	DS	OF
00002088				1741+	DROP	R5
00002088	99999900 18446744			1742	DC	XL16' 9999990018446744073709551615000C'
00002090	07370955 1615000C					
00002098	5A7E37BE 1E05A6B0			1743	DC	XL16' 5A7E37BE1E05A6B04C816BCDBFFFFFO0'
000020A0	4C816BCD BFFFFFO0					
				1744		
				1745		
				1746 * +1. 25		
				1747	VRR_J	VCSPH, 1, 1
000020A8				1748+	DS	OFD
000020A8		000020A8		1749+	USING	*, R5
000020A8	000020C8			1750+T42	DC	A(X42)
000020AC	002A			1751+	DC	H' 42'
000020AE	00			1752+	DC	X' 00'
000020AF	01			1753+	DC	HL1' 1'
000020B0	01			1754+V3_42	DC	HL1' 1'
000020B4	000020F8			1755+V2_42	DC	A(RE42+16)
000020B8	E5C3E2D7	C8404040		1756+	DC	CL8' VCSPH'
000020C0	00000010			1757+	DC	A(16)
000020C4	000020E8			1758+	DC	A(RE42)
				1759+*		
000020C8				1760+X42	DS	OF
000020C8	E710 8F14 0006	00001114		1761+	VL	V1, V1FUDGE
000020CE	E320 500C 0014	000020B4		1762+	LGF	R2, V2_42
000020D4	E722 0000 0006	00000000		1763+	VL	V2, 0(R2)
000020DA	E730 5008 7000	000020B0		1764+	VLEB	V3, V3_42, 7
000020E0	E612 3010 007D			1765+	VCSPH	V1, V2, V3, 1
000020E6	07FB			1766+	BR	R11
000020E8				1767+RE42	DS	OF
000020E8				1768+	DROP	R5
000020E8	00000000 00000000			1769	DC	XL16' 0000000000000000000000000000000013C'
000020F0	00000000 0000013C					
000020F8	41140000 00000000			1770	DC	XL16' 4114000000000000330000000000000000000000'
00002100	33000000 00000000					
				1771		
				1772 * +1. 5		
00002108				1773	VRR_J	VCSPH, 1, 1
00002108		00002108		1774+	DS	OFD
00002108	00002128			1775+	USING	*, R5
0000210C	002B			1776+T43	DC	A(X43)
0000210E	00			1777+	DC	H' 43'
				1778+	DC	X' 00'

LOC	OBJECT CODE	ADDR1	ADDR2	STM		
0000210F	01			1779+	DC	HL1' 1'
00002110	01			1780+V3_43	DC	HL1' 1'
00002114	00002158			1781+V2_43	DC	A(RE43+16)
00002118	E5C3E2D7 C8404040			1782+	DC	CL8' VCSPH'
00002120	00000010			1783+	DC	A(16)
00002124	00002148			1784+	DC	A(RE43)
				1785+*		
00002128				1786+X43	DS	OF
00002128	E710 8F14 0006	00001114		1787+	VL	V1, V1FUDGE
0000212E	E320 500C 0014	00002114		1788+	LGF	R2, V2_43
00002134	E722 0000 0006	00000000		1789+	VL	V2, 0(R2)
0000213A	E730 5008 7000	00002110		1790+	VLEB	V3, V3_43, 7
00002140	E612 3010 007D			1791+	VCSPH	V1, V2, V3, 1
00002146	07FB			1792+	BR	R11
00002148				1793+RE43	DS	OF
00002148				1794+	DROP	R5
00002148	00000000 00000000			1795	DC	XL16' 0000000000000000000000000000000015C'
00002150	00000000 0000015C			1796	DC	XL16' 41180000000000003300000000000000'
00002158	41180000 00000000					
00002160	33000000 00000000					
				1797		
				1798 * +1. 75		
				1799	VRR_J	VCSPH, 1, 1
00002168				1800+	DS	OFD
00002168		00002168		1801+	USING	*, R5
00002168	00002188			1802+T44	DC	A(X44)
0000216C	002C			1803+	DC	H' 44'
0000216E	00			1804+	DC	X' 00'
0000216F	01			1805+	DC	HL1' 1'
00002170	01			1806+V3_44	DC	HL1' 1'
00002174	000021B8			1807+V2_44	DC	A(RE44+16)
00002178	E5C3E2D7 C8404040			1808+	DC	CL8' VCSPH'
00002180	00000010			1809+	DC	A(16)
00002184	000021A8			1810+	DC	A(RE44)
				1811+*		
00002188				1812+X44	DS	OF
00002188	E710 8F14 0006	00001114		1813+	VL	V1, V1FUDGE
0000218E	E320 500C 0014	00002174		1814+	LGF	R2, V2_44
00002194	E722 0000 0006	00000000		1815+	VL	V2, 0(R2)
0000219A	E730 5008 7000	00002170		1816+	VLEB	V3, V3_44, 7
000021A0	E612 3010 007D			1817+	VCSPH	V1, V2, V3, 1
000021A6	07FB			1818+	BR	R11
000021A8				1819+RE44	DS	OF
000021A8				1820+	DROP	R5
000021A8	00000000 00000000			1821	DC	XL16' 0000000000000000000000000000000018C'
000021B0	00000000 0000018C			1822	DC	XL16' 411C0000000000003300000000000000'
000021B8	411C0000 00000000					
000021C0	33000000 00000000					
				1823		
000021C8	00000000			1824	DC	F' 0'
000021CC	00000000			1825	DC	F' 0'
				1826 *		
				1827 * table of pointers to individual tests		
				1828 *		
000021D0				1829 E6TESTS	DS	OF
				1830	PTTABLE	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	DS	OF	
000021D0				1831+TTABLE			
000021D0	00001148			1832+	DC	A(T1)	TEST &CUR
000021D4	000011A8			1833+	DC	A(T2)	TEST &CUR
000021D8	00001208			1834+	DC	A(T3)	TEST &CUR
000021DC	00001268			1835+	DC	A(T4)	TEST &CUR
000021E0	000012C8			1836+	DC	A(T5)	TEST &CUR
000021E4	00001328			1837+	DC	A(T6)	TEST &CUR
000021E8	00001388			1838+	DC	A(T7)	TEST &CUR
000021EC	000013E8			1839+	DC	A(T8)	TEST &CUR
000021F0	00001448			1840+	DC	A(T9)	TEST &CUR
000021F4	000014A8			1841+	DC	A(T10)	TEST &CUR
000021F8	00001508			1842+	DC	A(T11)	TEST &CUR
000021FC	00001568			1843+	DC	A(T12)	TEST &CUR
00002200	000015C8			1844+	DC	A(T13)	TEST &CUR
00002204	00001628			1845+	DC	A(T14)	TEST &CUR
00002208	00001688			1846+	DC	A(T15)	TEST &CUR
0000220C	000016E8			1847+	DC	A(T16)	TEST &CUR
00002210	00001748			1848+	DC	A(T17)	TEST &CUR
00002214	000017A8			1849+	DC	A(T18)	TEST &CUR
00002218	00001808			1850+	DC	A(T19)	TEST &CUR
0000221C	00001868			1851+	DC	A(T20)	TEST &CUR
00002220	000018C8			1852+	DC	A(T21)	TEST &CUR
00002224	00001928			1853+	DC	A(T22)	TEST &CUR
00002228	00001988			1854+	DC	A(T23)	TEST &CUR
0000222C	000019E8			1855+	DC	A(T24)	TEST &CUR
00002230	00001A48			1856+	DC	A(T25)	TEST &CUR
00002234	00001AA8			1857+	DC	A(T26)	TEST &CUR
00002238	00001B08			1858+	DC	A(T27)	TEST &CUR
0000223C	00001B68			1859+	DC	A(T28)	TEST &CUR
00002240	00001BC8			1860+	DC	A(T29)	TEST &CUR
00002244	00001C28			1861+	DC	A(T30)	TEST &CUR
00002248	00001C88			1862+	DC	A(T31)	TEST &CUR
0000224C	00001CE8			1863+	DC	A(T32)	TEST &CUR
00002250	00001D48			1864+	DC	A(T33)	TEST &CUR
00002254	00001DA8			1865+	DC	A(T34)	TEST &CUR
00002258	00001E08			1866+	DC	A(T35)	TEST &CUR
0000225C	00001E68			1867+	DC	A(T36)	TEST &CUR
00002260	00001EC8			1868+	DC	A(T37)	TEST &CUR
00002264	00001F28			1869+	DC	A(T38)	TEST &CUR
00002268	00001F88			1870+	DC	A(T39)	TEST &CUR
0000226C	00001FE8			1871+	DC	A(T40)	TEST &CUR
00002270	00002048			1872+	DC	A(T41)	TEST &CUR
00002274	000020A8			1873+	DC	A(T42)	TEST &CUR
00002278	00002108			1874+	DC	A(T43)	TEST &CUR
0000227C	00002168			1875+	DC	A(T44)	TEST &CUR
				1876+*			
00002280	00000000			1877+	DC	A(0)	END OF TABLE
00002284	00000000			1878+	DC	A(0)	
				1879			
00002288	00000000			1880	DC	F' 0'	END OF TABLE
0000228C	00000000			1881	DC	F' 0'	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				1883 ****	*****	*****
				1884 *	Register equates	
				1885 ****	*****	*****
	00000000	00000001	1887 R0	EQU	0	
	00000001	00000001	1888 R1	EQU	1	
	00000002	00000001	1889 R2	EQU	2	
	00000003	00000001	1890 R3	EQU	3	
	00000004	00000001	1891 R4	EQU	4	
	00000005	00000001	1892 R5	EQU	5	
	00000006	00000001	1893 R6	EQU	6	
	00000007	00000001	1894 R7	EQU	7	
	00000008	00000001	1895 R8	EQU	8	
	00000009	00000001	1896 R9	EQU	9	
	0000000A	00000001	1897 R10	EQU	10	
	0000000B	00000001	1898 R11	EQU	11	
	0000000C	00000001	1899 R12	EQU	12	
	0000000D	00000001	1900 R13	EQU	13	
	0000000E	00000001	1901 R14	EQU	14	
	0000000F	00000001	1902 R15	EQU	15	
				1904 ****	*****	*****
				1905 *	Register equates	
				1906 ****	*****	*****
	00000000	00000001	1908 FPR0	EQU	0	
	00000001	00000001	1909 FPR1	EQU	1	
	00000002	00000001	1910 FPR2	EQU	2	
	00000003	00000001	1911 FPR3	EQU	3	
	00000004	00000001	1912 FPR4	EQU	4	
	00000005	00000001	1913 FPR5	EQU	5	
	00000006	00000001	1914 FPR6	EQU	6	
	00000007	00000001	1915 FPR7	EQU	7	
	00000008	00000001	1916 FPR8	EQU	8	
	00000009	00000001	1917 FPR9	EQU	9	
	0000000A	00000001	1918 FPR10	EQU	10	
	0000000B	00000001	1919 FPR11	EQU	11	
	0000000C	00000001	1920 FPR12	EQU	12	
	0000000D	00000001	1921 FPR13	EQU	13	
	0000000E	00000001	1922 FPR14	EQU	14	
	0000000F	00000001	1923 FPR15	EQU	15	
				1925 ****	*****	*****
				1926 *	Register equates	
				1927 ****	*****	*****
	00000000	00000001	1929 V0	EQU	0	
	00000001	00000001	1930 V1	EQU	1	
	00000002	00000001	1931 V2	EQU	2	
	00000003	00000001	1932 V3	EQU	3	
	00000004	00000001	1933 V4	EQU	4	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
		00000005	00000001	1934 V5	EQU	5
		00000006	00000001	1935 V6	EQU	6
		00000007	00000001	1936 V7	EQU	7
		00000008	00000001	1937 V8	EQU	8
		00000009	00000001	1938 V9	EQU	9
		0000000A	00000001	1939 V10	EQU	10
		0000000B	00000001	1940 V11	EQU	11
		0000000C	00000001	1941 V12	EQU	12
		0000000D	00000001	1942 V13	EQU	13
		0000000E	00000001	1943 V14	EQU	14
		0000000F	00000001	1944 V15	EQU	15
		00000010	00000001	1945 V16	EQU	16
		00000011	00000001	1946 V17	EQU	17
		00000012	00000001	1947 V18	EQU	18
		00000013	00000001	1948 V19	EQU	19
		00000014	00000001	1949 V20	EQU	20
		00000015	00000001	1950 V21	EQU	21
		00000016	00000001	1951 V22	EQU	22
		00000017	00000001	1952 V23	EQU	23
		00000018	00000001	1953 V24	EQU	24
		00000019	00000001	1954 V25	EQU	25
		0000001A	00000001	1955 V26	EQU	26
		0000001B	00000001	1956 V27	EQU	27
		0000001C	00000001	1957 V28	EQU	28
		0000001D	00000001	1958 V29	EQU	29
		0000001E	00000001	1959 V30	EQU	30
		0000001F	00000001	1960 V31	EQU	31
				1961		
				1962		END

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RE29	F	00001C08	4	1418	1406 1409
RE3	F	00001248	4	722	710 713
RE30	F	00001C68	4	1444	1432 1435
RE31	F	00001CC8	4	1470	1458 1461
RE32	F	00001D28	4	1496	1484 1487
RE33	F	00001D88	4	1525	1513 1516
RE34	F	00001DE8	4	1552	1540 1543
RE35	F	00001E48	4	1578	1566 1569
RE36	F	00001EA8	4	1605	1593 1596
RE37	F	00001F08	4	1632	1620 1623
RE38	F	00001F68	4	1659	1647 1650
RE39	F	00001FC8	4	1686	1674 1677
RE4	F	000012A8	4	748	736 739
RE40	F	00002028	4	1713	1701 1704
RE41	F	00002088	4	1740	1728 1731
RE42	F	000020E8	4	1767	1755 1758
RE43	F	00002148	4	1793	1781 1784
RE44	F	000021A8	4	1819	1807 1810
RE5	F	00001308	4	775	763 766
RE6	F	00001368	4	802	790 793
RE7	F	000013C8	4	829	817 820
RE8	F	00001428	4	855	843 846
RE9	F	00001488	4	881	869 872
READDR	A	0000001C	4	556	234
REG2LOW	U	000000DD	1	475	
REG2PATT	U	AABBCCDD	1	474	
RELEN	A	00000018	4	555	
RPTDWSAV	D	000004D8	8	399	388 390
RPTERROR	I	000004AE	4	383	313 355
RPTSAVE	F	000004CC	4	396	383 393
RPTSVR5	F	000004D0	4	397	384 392
SCALE	U	00000008	1	552	251 304 347
SKL0001	U	0000006B	1	188	204
SKT0001	C	0000022A	26	185	188 205
SVOLDPSW	U	00000140	0	123	
T1	A	00001148	4	653	1832
T10	A	000014A8	4	890	1841
T11	A	00001508	4	919	1842
T12	A	00001568	4	945	1843
T13	A	000015C8	4	971	1844
T14	A	00001628	4	998	1845
T15	A	00001688	4	1025	1846
T16	A	000016E8	4	1052	1847
T17	A	00001748	4	1079	1848
T18	A	000017A8	4	1105	1849
T19	A	00001808	4	1131	1850
T2	A	000011A8	4	679	1833
T20	A	00001868	4	1157	1851
T21	A	000018C8	4	1186	1852
T22	A	00001928	4	1213	1853
T23	A	00001988	4	1239	1854
T24	A	000019E8	4	1266	1855
T25	A	00001A48	4	1293	1856
T26	A	00001AA8	4	1320	1857
T27	A	00001B08	4	1347	1858
T28	A	00001B68	4	1374	1859

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES																
T29	A	00001BC8	4	1401	1860																
T3	A	00001208	4	705	1834																
T30	A	00001C28	4	1427	1861																
T31	A	00001C88	4	1453	1862																
T32	A	00001CE8	4	1479	1863																
T33	A	00001D48	4	1508	1864																
T34	A	00001DA8	4	1535	1865																
T35	A	00001E08	4	1561	1866																
T36	A	00001E68	4	1588	1867																
T37	A	00001EC8	4	1615	1868																
T38	A	00001F28	4	1642	1869																
T39	A	00001F88	4	1669	1870																
T4	A	00001268	4	731	1835																
T40	A	00001FE8	4	1696	1871																
T41	A	00002048	4	1723	1872																
T42	A	000020A8	4	1750	1873																
T43	A	00002108	4	1776	1874																
T44	A	00002168	4	1802	1875																
T5	A	000012C8	4	758	1836																
T6	A	00001328	4	785	1837																
T7	A	00001388	4	812	1838																
T8	A	000013E8	4	838	1839																
T9	A	00001448	4	864	1840																
TESTING	F	00001004	4	486	225																
TNUM	H	00000004	2	549	224	288	331														
TSUB	A	00000000	4	548	227																
TTABLE	F	000021D0	4	1831																	
V0	U	00000000	1	1929																	
V1	U	00000001	1	1930	230	278	664	668	690	694	716	720	742	746	769	773	796				
					800	823	827	849	853	875	879	901	905	930	934	956	960				
					982	986	1009	1013	1036	1040	1063	1067	1090	1094	1116	1120	1142				
					1146	1168	1172	1197	1201	1224	1228	1250	1254	1277	1281	1304	1308				
					1331	1335	1358	1362	1385	1389	1412	1416	1438	1442	1464	1468	1490				
					1494	1519	1523	1546	1550	1572	1576	1599	1603	1626	1630	1653	1657				
					1680	1684	1707	1711	1734	1738	1761	1765	1787	1791	1813	1817					
V10	U	0000000A	1	1939																	
V11	U	0000000B	1	1940																	
V12	U	0000000C	1	1941																	
V13	U	0000000D	1	1942																	
V14	U	0000000E	1	1943																	
V15	U	0000000F	1	1944																	
V16	U	00000010	1	1945																	
V17	U	00000011	1	1946																	
V18	U	00000012	1	1947																	
V19	U	00000013	1	1948																	
V1FUDGE	X	00001114	16	539	664	690	716	742	769	796	823	849	875	901	930	956	982				
					1009	1036	1063	1090	1116	1142	1168	1197	1224	1250	1277	1304	1331				
					1358	1385	1412	1438	1464	1490	1519	1546	1572	1599	1626	1653	1680				
					1707	1734	1761	1787	1813												
V1INPUT	X	00001124	16	540																	
V10OUTPUT	X	000010F4	16	537	230	235	668	692	694	718	720	744	746	771	773	798	800				
					825	827	851	853	877	879	903	905	932	934	958	960	984				
					986	1011	1013	1038	1040	1065	1067	1092	1094	1118	1120	1144	1146				
					1170	1172	1199	1201	1226	1228	1252	1254	1279	1281	1306	1308	1333				
					1335	1360	1362	1387	1389	1414	1416	1440	1442	1466	1468	1492	1494				

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V2_9	A	00001454	4	869	876
V3	U	00000003	1	1932	667 827 1012 1172 1361 1523 1710
					668 852 853 1039 1201 1388 1550 1737
					693 878 1040 1227 1389 1575 1738
					694 879 1066 1228 1415 1576 1764
					719 904 1067 1253 1416 1602 1765
					720 905 1093 1254 1441 1603 1790
					745 933 1094 1280 1442 1467 1468
					746 934 1119 1281 1442 1467 1493
					772 959 1120 1307 1442 1467 1494
					773 960 1145 1308 1334 1335 1522
					799 1146 1334 1335 1493 1494 1522
					800 985 986 1171 1335 1657 1683 1684
V30	U	0000001E	1	1959	
V31	U	0000001F	1	1960	
V3_1	U	00001150	1	657	667
V3_10	U	000014B0	1	894	904
V3_11	U	00001510	1	923	933
V3_12	U	00001570	1	949	959
V3_13	U	000015D0	1	975	985
V3_14	U	00001630	1	1002	1012
V3_15	U	00001690	1	1029	1039
V3_16	U	000016F0	1	1056	1066
V3_17	U	00001750	1	1083	1093
V3_18	U	000017B0	1	1109	1119
V3_19	U	00001810	1	1135	1145
V3_2	U	000011B0	1	683	693
V3_20	U	00001870	1	1161	1171
V3_21	U	000018D0	1	1190	1200
V3_22	U	00001930	1	1217	1227
V3_23	U	00001990	1	1243	1253
V3_24	U	000019F0	1	1270	1280
V3_25	U	00001A50	1	1297	1307
V3_26	U	00001AB0	1	1324	1334
V3_27	U	00001B10	1	1351	1361
V3_28	U	00001B70	1	1378	1388
V3_29	U	00001BD0	1	1405	1415
V3_3	U	00001210	1	709	719
V3_30	U	00001C30	1	1431	1441
V3_31	U	00001C90	1	1457	1467
V3_32	U	00001CF0	1	1483	1493
V3_33	U	00001D50	1	1512	1522
V3_34	U	00001DB0	1	1539	1549
V3_35	U	00001E10	1	1565	1575
V3_36	U	00001E70	1	1592	1602
V3_37	U	00001ED0	1	1619	1629
V3_38	U	00001F30	1	1646	1656
V3_39	U	00001F90	1	1673	1683
V3_4	U	00001270	1	735	745
V3_40	U	00001FF0	1	1700	1710
V3_41	U	00002050	1	1727	1737
V3_42	U	000020B0	1	1754	1764
V3_43	U	00002110	1	1780	1790
V3_44	U	00002170	1	1806	1816
V3_5	U	000012D0	1	762	772
V3_6	U	00001330	1	789	799
V3_7	U	00001390	1	816	826
V3_8	U	000013F0	1	842	852
V3_9	U	00001450	1	868	878
V4	U	00000004	1	1933	
V5	U	00000005	1	1934	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V6	U	00000006	1	1935	
V7	U	00000007	1	1936	
V8	U	00000008	1	1937	
V9	U	00000009	1	1938	
X0001	U	000002C8	1	194	182 195
X1	F	00001168	4	663	653
X10	F	000014C8	4	900	890
X11	F	00001528	4	929	919
X12	F	00001588	4	955	945
X13	F	000015E8	4	981	971
X14	F	00001648	4	1008	998
X15	F	000016A8	4	1035	1025
X16	F	00001708	4	1062	1052
X17	F	00001768	4	1089	1079
X18	F	000017C8	4	1115	1105
X19	F	00001828	4	1141	1131
X2	F	000011C8	4	689	679
X20	F	00001888	4	1167	1157
X21	F	000018E8	4	1196	1186
X22	F	00001948	4	1223	1213
X23	F	000019A8	4	1249	1239
X24	F	00001A08	4	1276	1266
X25	F	00001A68	4	1303	1293
X26	F	00001AC8	4	1330	1320
X27	F	00001B28	4	1357	1347
X28	F	00001B88	4	1384	1374
X29	F	00001BE8	4	1411	1401
X3	F	00001228	4	715	705
X30	F	00001C48	4	1437	1427
X31	F	00001CA8	4	1463	1453
X32	F	00001D08	4	1489	1479
X33	F	00001D68	4	1518	1508
X34	F	00001DC8	4	1545	1535
X35	F	00001E28	4	1571	1561
X36	F	00001E88	4	1598	1588
X37	F	00001EE8	4	1625	1615
X38	F	00001F48	4	1652	1642
X39	F	00001FA8	4	1679	1669
X4	F	00001288	4	741	731
X40	F	00002008	4	1706	1696
X41	F	00002068	4	1733	1723
X42	F	000020C8	4	1760	1750
X43	F	00002128	4	1786	1776
X44	F	00002188	4	1812	1802
X5	F	000012E8	4	768	758
X6	F	00001348	4	795	785
X7	F	000013A8	4	822	812
X8	F	00001408	4	848	838
X9	F	00001468	4	874	864
XC0001	U	000002F0	1	208	200
XCHECK	U	0000032E	1	249	232
XCPLINE	C	00001054	13	511	520 312
XCPLNG	U	00000053	1	520	311
XCPMA	C	00001094	2	516	301
XCPNAME	C	00001083	8	514	294
XCPSCALE	C	000010A3	3	518	308

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
XCPTNUM	C	00001061	3	512	292
XCR01	H	00000366	2	271	265
XCR02	H	0000036C	2	277	269
XCR15	F	00000420	8	322	310
XCRESULT	X	000003F0	16	319	315
XCV1	X	00000400	16	320	
XCV2	X	00000410	16	321	257
ZVE6TST	J	00000000	8848	120	123
=A(E6TESTS)	A	000005D8	4	462	215
=AL2(L' MSGMSG)	R	000005E2	2	465	411
=F' 1'	F	000005DC	4	463	361
=F' 128'	F	000005D4	4	461	199
=H' 0'	H	000005E0	2	464	406

MACRO DEFN REFERENCES

FCHECK	72	181																
PTTABLE	613	1830																
VRR_J	572	650 1102 1558	676 1128 1585	702 1154 1612	728 1183 1639	755 1210 1666	782 1236 1693	809 1263 1720	835 1290 1747	861 1317 1773	887 1344 1799	916 1371	942 1398	968 1424	995 1450	1022 1476	1049 1476	1076 1532

DESC	SYMBOL	SIZE	POS	ADDR
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Entry: 0

Image	IMAGE	8848	0000-228F	0000-228F
Region		8848	0000-228F	0000-228F
CSECT	ZVE6TST	8848	0000-228F	0000-228F

STMT	FILE NAME
1	/home/tn529/sharedvfp/tests/zvector-e6-19-VCSPH.asm
** NO ERRORS FOUND **	