

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
2				*****
3				*
4				* TRTR instruction tests
5				*
6				* NOTE: This test is based the CLCL-et-al Test
7				* modified to only test the TRTR instruction.
8				*
9				* James Wekel November 2022
10				*****
12				*****
13				*
14				* TRTR basic instruction tests
15				*
16				*****
17				* This program tests proper functioning of the TRTR
18				* instructions. Specification exceptions are not tested.
19				*
20				* PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
21				* obvious coding errors. None of the tests are thorough. They are
22				* NOT designed to test all aspects of the TRTR instruction.
23				*
24				*****
25				*
26				* Example Hercules Testcase:
27				*
28				* *Testcase TRTR-01-basic (Test TRTR instructions)
29				*
30				* # -----
31				* # This tests only the basic function of the TRTR instruction.
32				* # Specification Exceptions are NOT tested.
33				* # -----
34				* mainsize 16
35				* numcpu 1
36				* sysclear
37				* archlvl z/Arch
38				*
39				* loadcore "\$(testpath)/TRTR-01-basic" 0x0
40				*
41				* runtest 1
42				*
43				* *Done
44				*
45				*****

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				47	*****		
				48	*	Low Core Definitions	
				49	*****		
				50	*		
00000000		00000000	00000EF7	51	TRTR1TST	START 0	
		00000000		52		USING TRTR1TST,R0	Low core addressability
00000000		00000000	000001A0	54	ORG	TRTR1TST+X'1A0'	z/Architecure RESTART PSW
000001A0	00000001 80000000			55	DC	X'0000000180000000'	
000001A8	00000000 00000200			56	DC	AD(BEGIN)	
000001B0		000001B0	000001D0	58	ORG	TRTR1TST+X'1D0'	z/Architecure PROGRAM CHECK PSW
000001D0	00020001 80000000			59	DC	X'0002000180000000'	
000001D8	00000000 0000DEAD			60	DC	AD(X'DEAD')	
000001E0		000001E0	00000200	62	ORG	TRTR1TST+X'200'	Start of actual test program...

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				64	*****	
				65	*	The actual "TRTR1TST" program itself...
				66	*****	
				67	*	
				68	*	Architecture Mode: z/Arch
				69	*	Register Usage:
				70	*	
				71	*	R0 (work)
				72	*	R1 TRTR - Function-Code Address
				73	*	R2 TRTR - Function-Code
				74	*	R3 TRTR - First-Operand Address
				75	*	R4 TRTR - First-Operand Length
				76	*	R5 TRTR - Function-Code Table Address
				77	*	R6-R7 (work)
				78	*	R8 First base register
				79	*	R9 Second base register
				80	*	R10-R12 (work)
				81	*	R13 Testing control table - base current entry
				82	*	R14 Subroutine call
				83	*	R15 Secondary Subroutine call or work
				84	*	
				85	*****	
00000200		00000200		87	USING	BEGIN,R8 FIRST Base Register
00000200		00001200		88	USING	BEGIN+4096,R9 SECOND Base Register
00000200	0580			90	BEGIN	BALR R8,0 Initalize FIRST base register
00000202	0680			91		BCTR R8,0 Initalize FIRST base register
00000204	0680			92		BCTR R8,0 Initalize FIRST base register
00000206	4190 8800		00000800	94	LA	R9,2048(,R8) Initalize SECOND base register
0000020A	4190 9800		00000800	95	LA	R9,2048(,R9) Initalize SECOND base register
				96	*	
				97	**	Run the tests...
				98	*	
0000020E	45E0 8302		00000502	99	BAL	R14,TEST01 Test TRTR instruction
				100	*	
				102	*****	
				103	*	Test for normal or unexpected test completion...
				104	*****	
00000212	9526 8200		00000400	106	CLI	TESTNUM,X'26' Did we end on expected test?
00000216	4770 83C0		000005C0	107	BNE	FAILTEST No?! Then FAIL the test!
0000021A	9502 8201		00000401	109	CLI	SUBTEST,X'02' Did we end on expected SUB-test?
0000021E	4770 83C0		000005C0	110	BNE	FAILTEST No?! Then FAIL the test!
00000222	47F0 83A8		000005A8	112	B	E0J Yes, then normal completion!

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				114 *****
				115 * Fixed test storage locations ...
				116 *****
00000226		00000226	00000400	118 ORG BEGIN+X'200'
				119
00000400				120 TESTADDR DS 0D Where test/subtest numbers will go
00000400	99			121 TESTNUM DC X'99' Test number of active test
00000401	99			122 SUBTEST DC X'99' Active test sub-test number
00000402		00000402	00000502	124 ORG ++X'100'

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				126	*****	
				127	*	TEST01 Test TRTR instruction
				128	*****	
00000502	9201 8200		00000400	130	TEST01 MVI	TESTNUM,X'01'
				131		
00000506	41D0 83C8		000005C8	132	LA	R13,TRTRCTL Point R6 --> testing control table
0000050A		00000000		133	USING	TRTRTEST,R13 What each table entry looks like
				134		
		0000050A	00000001	135	TST1LOOP EQU	*
0000050A	4360 D000		00000000	136	IC	R6,TNUM Set test number
0000050E	4260 8200		00000400	137	STC	R6,TESTNUM
				138	*	
				139	**	Initialize operand data (move data to testing address)
				140	*	
00000512	58A0 D01C		0000001C	141	L	R10,OP1WHERE Where to move operand-1 data to
00000516	58B0 D008		00000008	142	L	R11,OP1LEN operand-1 length
0000051A	50B0 D020		00000020	143	ST	R11,OP1WLEN and save for later
0000051E	5860 D004		00000004	144	L	R6,OP1DATA Where op1 data is right now
00000522	5870 D008		00000008	145	L	R7,OP1LEN How much of it there is
00000526	0EA6			146	MVCL	R10,R6
				147	*	
00000528	58A0 D024		00000024	148	L	R10,OP2WHERE Where to move operand-2 data to
0000052C	58B0 D010		00000010	149	L	R11,OP2LEN How much of it there is
00000530	5860 D00C		0000000C	150	L	R6,OP2DATA Where op2 data is right now
00000534	5870 D010		00000010	151	L	R7,OP2LEN How much of it there is
00000538	0EA6			152	MVCL	R10,R6
				154	*	Setup for TRTR instruction: adjust OP address
0000053A	58B0 D028		00000028	156	L	R11,FAILMASK (failure CC)
0000053E	89B0 0004		00000004	157	SLL	R11,4 (shift to BC instr CC position)
00000542	9200 8201		00000401	159	MVI	SUBTEST,X'00' (primary TRTR)
00000546	9815 D014		00000014	161	LM	R1,R5,OPSWHERE get TRTR input; set OP addr to end
0000054A	1A34			162	AR	R3,R4 add OP length -1
0000054C	0630			163	BCTR	R3,0

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
165 * Execute TRTR instruction and check for expected condition code							
0000054E	1864			167	LR	R6,R4	get op-1 length -1 for EX
00000550	0660			168	BCTR	R6,0	
00000552	4460 838E		0000058E	169	EX	R6,TRTRES	'TRTR 0(0,R3),0(R5)'
00000556	44B0 838A		0000058A	171	EX	R11,TRTRBC	fail if...
				173 **	Verify R1,R2 contain (or still contain!) expected values		
0000055A	98AC D02C		0000002C	175	LM	R10,R12,ENDREGS	
0000055E	9201 8201		00000401	177	MVI	SUBTEST,X'01'	(R2 result - op1 found addr)
00000562	151A			178	CLR	R1,R10	R2 correct?
00000564	4770 8384		00000584	179	BNE	TRTRFAIL	No, FAILTEST!
00000568	9202 8201		00000401	181	MVI	SUBTEST,X'02'	(R3 result - op1 remaining len)
0000056C	152B			182	CLR	R2,R11	R3 correct
0000056E	4770 8384		00000584	183	BNE	TRTRFAIL	No, FAILTEST!
00000572	41D0 D034		00000034	185	LA	R13,TRTRNEXT	Go on to next table entry
00000576	D503 83C4 D000	000005C4	00000000	186	CLC	=F'0',0(R13)	End of table?
0000057C	4770 830A		0000050A	187	BNE	TST1LOOP	No, loop...
00000580	47F0 8388		00000588	188	B	TRTRDONE	Done! (success!)
00000584	41E0 83C0		000005C0	190	TRTRFAIL	LA R14,FAILTEST	Unexpected results!
00000588	07FE			191	TRTRDONE	BR R14	Return to caller or FAILTEST
0000058A	4700 8384		00000584	193	TRTRBC	BC 0,TRTRFAIL	(fail if unexpected condition code)
0000058E	D000 3000 5000	00000000	00000000	195	TRTRES	TRTR 0(0,R3),0(R5)	
				196			
00000594				197	DROP	R13	
00000594				198	DROP	R15	
00000594	00000200			199	USING	BEGIN,R8	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				201	*****
				202	* Normal completion or Abnormal termination PSWs
				203	*****
00000598	00020001 80000000			205	EJPSW DC 0D'0',X'0002000180000000',AD(0)
000005A8	B2B2 8398		00000598	207	EJ LPSWE EJPSW Normal completion
000005B0	00020001 80000000			209	FAILPSW DC 0D'0',X'0002000180000000',AD(X'BAD')
000005C0	B2B2 83B0		000005B0	211	FAILTEST LPSWE FAILPSW Abnormal termination
				213	*****
				214	* Working Storage
				215	*****
000005C4				217	LTORG , Literals pool
000005C4	00000000			218	=F'0'
	00000400	00000001		220	K EQU 1024 One KB
	00001000	00000001		221	PAGE EQU (4*K) Size of one page
	00004000	00000001		222	K16 EQU (16*K) 16 KB
	00008000	00000001		223	K32 EQU (32*K) 32 KB
	00010000	00000001		224	K64 EQU (64*K) 64 KB
	00100000	00000001		225	MB EQU (K*K) 1 MB

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
		00000000	00000EF7	227 TRTR1TST CSECT ,	
				229 *****	
				230 * TRTRTEST DSECT	
				231 *****	
				233 TRTRTEST DSECT ,	
00000000	00			234 TNUM DC X'00'	TRTR table Number
00000001	00			235 DC X'00'	
00000002	00			236 DC X'00'	
00000003	00			237 DC X'00'	
				239 OP1DATA DC A(0)	Pointer to Operand-1 data
00000004	00000000			240 OP1LEN DC F'0'	How much data is there - 1
00000008	00000000			241 OP2DATA DC A(0)	Pointer to FC table data
0000000C	00000000			242 OP2LEN DC F'0'	How much data is there - FC Table
		00000014	00000001	244 OPSWHERE EQU *	
00000014	00000000			245 GR1PATT DC A(0)	GR1 - Polluted Register pattern
00000018	00000000			246 GR2PATT DC A(0)	GR2 - Polluted Register pattern
0000001C	00000000			247 OP1WHERE DC A(0)	Where Operand-1 data should be placed
00000020	00000000			248 OP1WLEN DC F'0'	How much data is there - 1
00000024	00000000			249 OP2WHERE DC A(0)	Where FC Table data should be placed
				251 FAILMASK DC A(0)	Failure Branch on Condition mask
				253 *	Ending register values
0000002C	00000000			254 ENDREGS DC A(0)	GR1 - FC address
00000030	00000000			255 DC A(0)	GR2 - Function Code
		00000034	00000001	257 TRTRNEXT EQU *	Start of next table entry...
		AABBCCDD	00000001	259 REG2PATT EQU X'AABBCCDD'	Polluted Register pattern
		000000DD	00000001	260 REG2LOW EQU X'DD'	(last byte above)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
		00000000	00000EF7	262	TRTR1TST CSECT ,
				264	*****
				265	* TRTR Testing Control tables (ref: TRTRTEST DSECT)
				266	*****
000005C8				267	PRINT DATA
				268	TRTRCTL DC 0A(0) start of table
				270	*****
				271	* tests with CC=0
				272	*****
000005C8				274	CC0T1 DS 0F
000005C8	01			275	DC X'01' Test Num
000005C9	0000			276	DC X'00',X'00'
000005CB	00			277	DC X'00'
				278	*
000005CC	000008DC	00000001		279	DC A(TRTOP10),A(001) Source - Op 1 & length
000005D4	00000BDC	00000100		280	DC A(TRTOP20),A(256) Source - FC Table & length
				281	* Target -
000005DC	AABBCCDD	AABBCCDD		282	DC A(REG2PATT),A(REG2PATT) GR1, GR2
000005E4	00100000	00000000		283	DC A(1*MB+(0*K16)),A(0),A(2*MB+(0*K16)) Op1, Op1L, FCT
000005EC	00200000				
				284	*
000005F0	00000007			285	DC A(7) not CC0
000005F4	AABBCCDD	AABBCCDD		286	DC A(REG2PATT),A(REG2PATT) FC address, Code
000005FC				288	CC0T2 DS 0F
000005FC	02			289	DC X'02' Test Num
000005FD	0000			290	DC X'00',X'00'
000005FF	00			291	DC X'00'
				292	*
00000600	000008DC	00000004		293	DC A(TRTOP10),A(004) Source - Op 1 & length
00000608	00000BDC	00000100		294	DC A(TRTOP20),A(256) Source - FC Table & length
				295	* Target -
00000610	AABBCCDD	AABBCCDD		296	DC A(REG2PATT),A(REG2PATT) GR1, GR2
00000618	00104000	00000000		297	DC A(1*MB+(1*K16)),A(0),A(2*MB+(1*K16)) Op1, Op1L, FCT
00000620	00204000				
				298	*
00000624	00000007			299	DC A(7) not CC0
00000628	AABBCCDD	AABBCCDD		300	DC A(REG2PATT),A(REG2PATT) FC address, Code
00000630				302	CC0T3 DS 0F
00000630	03			303	DC X'03' Test Num
00000631	0000			304	DC X'00',X'00'
00000633	00			305	DC X'00'
				306	*
00000634	000008DC	00000040		307	DC A(TRTOP10),A(064) Source - Op 1 & length
0000063C	00000BDC	00000100		308	DC A(TRTOP20),A(256) Source - FC Table & length
				309	* Target -
00000644	AABBCCDD	AABBCCDD		310	DC A(REG2PATT),A(REG2PATT) GR1, GR2

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000064C	00108000 00000000			311	DC	A(1*MB+(2*K16)),A(0),A(2*MB+(2*K16))	Op1, Op1L, FCT
00000654	00208000			312 *			
00000658	00000007			313	DC	A(7)	not CC0
0000065C	AABBCCDD AABBCCDD			314	DC	A(REG2PATT),A(REG2PATT)	FC address, Code
00000664				316	CC0T4 DS	0F	
00000664	04			317	DC	X'04'	Test Num
00000665	0000			318	DC	X'00',X'00'	
00000667	00			319	DC	X'00'	
				320 *			
00000668	000008DC 00000100			321	DC	A(TRTOP10),A(256)	Source - Op 1 & length
00000670	00000BDC 00000100			322	DC	A(TRTOP20),A(256)	Source - FC Table & length
				323 *			Target -
00000678	AABBCCDD AABBCCDD			324	DC	A(REG2PATT),A(REG2PATT)	GR1, GR2
00000680	0010C000 00000000			325	DC	A(1*MB+(3*K16)),A(0),A(2*MB+(3*K16))	Op1, Op1L, FCT
00000688	0020C000			326 *			
0000068C	00000007			327	DC	A(7)	not CC0
00000690	AABBCCDD AABBCCDD			328	DC	A(REG2PATT),A(REG2PATT)	FC address, Code

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				331	*****			
				332	*	tests with CC=1		
				333	*****			
00000698				335	CC1T1	DS	0F	
00000698	11			336		DC	X'11'	
00000699	0000			337		DC	X'00',X'00'	
0000069B	00			338		DC	X'00'	
				339	*			
0000069C	000009DC	00000004		340		DC	A(TRTOP1F0),A(004)	
000006A4	00000CE8	00000100		341		DC	A(TRTOP2F0),A(256)	
				342	*		Source - Op 1 & length Source - FC Table & length Target -	
000006AC	AABBCCDD	AABBCCDD		343		DC	A(REG2PATT),A(REG2PATT)	
000006B4	00300000	00000000		344		DC	A(3*MB+(0*K16)),A(0),A(4*MB+(0*K16))	
000006BC	00400000						GR1, GR2 Op1, Op1L, FCT	
				345	*			
000006C0	0000000B			346		DC	A(11)	
000006C4	00300001	AABBCCF0		347		DC	A(3*MB+(0*K16)+1),XL4'AABBCCF0'	
							not CC1 FC address, Code	
000006CC				349	CC1T2	DS	0F	
000006CC	12			350		DC	X'12'	
000006CD	0000			351		DC	X'00',X'00'	
000006CF	00			352		DC	X'00'	
				353	*			
000006D0	000009DC	00000010		354		DC	A(TRTOP1F0),A(016)	
000006D8	00000CE8	00000100		355		DC	A(TRTOP2F0),A(256)	
				356	*		Source - Op 1 & length Source - FC Table & length Target -	
000006E0	AABBCCDD	AABBCCDD		357		DC	A(REG2PATT),A(REG2PATT)	
000006E8	00304000	00000000		358		DC	A(3*MB+(1*K16)),A(0),A(4*MB+(1*K16))	
000006F0	00404000						GR1, GR2 Op1, Op1L, FCT	
				359	*			
000006F4	0000000B			360		DC	A(11)	
000006F8	00304001	AABBCCF0		361		DC	A(3*MB+(1*K16)+1),XL4'AABBCCF0'	
							not CC1 FC address, Code	
00000700				363	CC1T3	DS	0F	
00000700	13			364		DC	X'13'	
00000701	0000			365		DC	X'00',X'00'	
00000703	00			366		DC	X'00'	
				367	*			
00000704	000009DC	00000100		368		DC	A(TRTOP1F0),A(256)	
0000070C	00000CE8	00000100		369		DC	A(TRTOP2F0),A(256)	
				370	*		Source - Op 1 & length Source - FC Table & length Target -	
00000714	AABBCCDD	AABBCCDD		371		DC	A(REG2PATT),A(REG2PATT)	
0000071C	00308000	00000000		372		DC	A(3*MB+(2*K16)),A(0),A(4*MB+(2*K16))	
00000724	00408000						GR1, GR2 Op1, Op1L, FCT	
				373	*			
00000728	0000000B			374		DC	A(11)	
0000072C	00308001	AABBCCF0		375		DC	A(3*MB+(2*K16)+1),XL4'AABBCCF0'	
							not CC1 FC address, Code	
				377	*		cross page tests	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00000734				379	CC1T4	DS	0F	
00000734	14			380		DC	X'14'	Test Num
00000735	0000			381		DC	X'00',X'00'	
00000737	00			382		DC	X'00'	
				383	*			
00000738	000009DC	00000010		384		DC	A(TRTOP1F0),A(016)	Source - Op 1 & length
00000740	00000CE8	00000100		385		DC	A(TRTOP2F0),A(256)	Source - FC Table & length
				386	*			Target -
00000748	AABBCCDD	AABBCCDD		387		DC	A(REG2PATT),A(REG2PATT)	GR1, GR2
00000750	0030BFF7	00000000		388		DC	A(3*MB+(3*K16)-9),A(0),A(4*MB+(3*K16)-9)	Op1, Op1L, FCT
00000758	0040BFF7							
				389	*			
0000075C	0000000B			390		DC	A(11)	not CC1
00000760	0030BFF8	AABBCCF0		391		DC	A(3*MB+(3*K16)-9+1),XL4'AABBCCF0'	FC address, Code
00000768				393	CC1T5	DS	0F	
00000768	15			394		DC	X'15'	Test Num
00000769	0000			395		DC	X'00',X'00'	
0000076B	00			396		DC	X'00'	
				397	*			
0000076C	000009DC	00000100		398		DC	A(TRTOP1F0),A(256)	Source - Op 1 & length
00000774	00000CE8	00000100		399		DC	A(TRTOP2F0),A(256)	Source - FC Table & length
				400	*			Target -
0000077C	AABBCCDD	AABBCCDD		401		DC	A(REG2PATT),A(REG2PATT)	GR1, GR2
00000784	0030FFF3	00000000		402		DC	A(3*MB+(4*K16)-13),A(0),A(4*MB+(4*K16)-29)	Op1,.., FCT
0000078C	0040FFE3							
				403	*			
00000790	0000000B			404		DC	A(11)	not CC1
00000794	0030FFF4	AABBCCF0		405		DC	A(3*MB+(4*K16)-13+1),XL4'AABBCCF0'	FC address, Code

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				408	*****			
				409	*	tests with CC=2		
				410	*****			
0000079C				412	CC2T1	DS	0F	
0000079C	21			413		DC	X'21'	
0000079D	0000			414		DC	X'00',X'00'	
0000079F	00			415		DC	X'00'	
				416	*			
000007A0	00000ADC	00000004		417		DC	A(TRTOP1F1),A(004)	
000007A8	00000DF0	00000100		418		DC	A(TRTOP8F1),A(256)	
				419	*		Source - Op 1 & length Source - FC Table & length Target -	
000007B0	AABBCCDD	AABBCCDD		420		DC	A(REG2PATT),A(REG2PATT)	
000007B8	00500000	00000000		421		DC	A(5*MB+(0*K16)),A(0),A(6*MB+(0*K16))	
000007C0	00600000						GR1, GR2 Op1, Op1L, FCT	
				422	*			
000007C4	0000000D			423		DC	A(13)	
000007C8	00500000	AABBCCF1		424		DC	A(5*MB+(0*K16)),XL4 'AABBCCF1'	
							not CC2 FC address, Code	
000007D0				426	CC2T2	DS	0F	
000007D0	22			427		DC	X'22'	
000007D1	0000			428		DC	X'00',X'00'	
000007D3	00			429		DC	X'00'	
				430	*			
000007D4	00000ADC	00000010		431		DC	A(TRTOP1F1),A(016)	
000007DC	00000DF0	00000100		432		DC	A(TRTOP8F1),A(256)	
				433	*		Source - Op 1 & length Source - FC Table & length Target -	
000007E4	AABBCCDD	AABBCCDD		434		DC	A(REG2PATT),A(REG2PATT)	
000007EC	00504000	00000000		435		DC	A(5*MB+(1*K16)),A(0),A(6*MB+(1*K16))	
000007F4	00604000						GR1, GR2 Op1, Op1L, FCT	
				436	*			
000007F8	0000000D			437		DC	A(13)	
000007FC	00504000	AABBCCF1		438		DC	A(5*MB+(1*K16)),XL4 'AABBCCF1'	
							not CC2 FC address, Code	
00000804				440	CC2T3	DS	0F	
00000804	23			441		DC	X'23'	
00000805	0000			442		DC	X'00',X'00'	
00000807	00			443		DC	X'00'	
				444	*			
00000808	00000ADC	00000100		445		DC	A(TRTOP1F1),A(256)	
00000810	00000DF0	00000100		446		DC	A(TRTOP8F1),A(256)	
				447	*		Source - Op 1 & length Source - FC Table & length Target -	
00000818	AABBCCDD	AABBCCDD		448		DC	A(REG2PATT),A(REG2PATT)	
00000820	00508000	00000000		449		DC	A(5*MB+(2*K16)),A(0),A(6*MB+(2*K16))	
00000828	00608000						GR1, GR2 Op1, Op1L, FCT	
				450	*			
0000082C	0000000D			451		DC	A(13)	
00000830	00508000	AABBCCF1		452		DC	A(5*MB+(2*K16)),XL4 'AABBCCF1'	
							not CC2 FC address, Code	
				454	*		cross page tests	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00000838				456	CC2T4	DS	0F
00000838	24			457		DC	X'24'
00000839	0000			458		DC	X'00',X'00'
0000083B	00			459		DC	X'00'
				460	*		
0000083C	00000ADC	00000010		461		DC	A(TRTOP1F1),A(016)
00000844	00000DF0	00000100		462		DC	A(TRTOP8F1),A(256)
				463	*		Source - Op 1 & length Source - FC Table & length Target -
0000084C	AABBCCDD	AABBCCDD		464		DC	A(REG2PATT),A(REG2PATT)
00000854	0050BFF7	00000000		465		DC	A(5*MB+(3*K16)-9),A(0),A(6*MB+(3*K16)-9)
0000085C	0060BFF7						GR1, GR2 Op1, Op1L, FCT
				466	*		
00000860	0000000D			467		DC	A(13)
00000864	0050BFF7	AABBCCF1		468		DC	A(5*MB+(3*K16)-9),XL4'AABBCCF1'
							not CC2 FC address, Code
0000086C				470	CC2T5	DS	0F
0000086C	25			471		DC	X'25'
0000086D	0000			472		DC	X'00',X'00'
0000086F	00			473		DC	X'00'
				474	*		
00000870	00000ADC	00000100		475		DC	A(TRTOP1F1),A(256)
00000878	00000DF0	00000100		476		DC	A(TRTOP8F1),A(256)
				477	*		Source - Op 1 & length Source - FC Table & length Target -
00000880	AABBCCDD	AABBCCDD		478		DC	A(REG2PATT),A(REG2PATT)
00000888	0050FFF3	00000000		479		DC	A(5*MB+(4*K16)-13),A(0),A(6*MB+(4*K16)-29)
00000890	0060FFE3						GR1, GR2 Op1,.., FCT
				480	*		
00000894	0000000D			481		DC	A(13)
00000898	0050FFF3	AABBCCF1		482		DC	A(5*MB+(4*K16)-13),XL4'AABBCCF1'
							not CC2 FC address, Code
000008A0				484	CC2T6	DS	0F
000008A0	26			485		DC	X'26'
000008A1	0000			486		DC	X'00',X'00'
000008A3	00			487		DC	X'00'
				488	*		
000008A4	00000ADC	00000100		489		DC	A(TRTOP1F1),A(256)
000008AC	00000DF0	00000100		490		DC	A(TRTOP8F1),A(256)
				491	*		Source - Op 1 & length Source - FC Table & length Target -
000008B4	AABBCCDD	AABBCCDD		492		DC	A(REG2PATT),A(REG2PATT)
000008BC	00513FFF	00000000		493		DC	A(5*MB+(5*K16)-1),A(0),A(6*MB+(5*K16)+29)
000008C4	0061401D						GR1, GR2 Op1,.., FCT
				494	*		
000008C8	0000000D			495		DC	A(13)
000008CC	00513FFF	AABBCCF1		496		DC	A(5*MB+(5*K16)-1),XL4'AABBCCF1'
							not CC2 FC address, Code
000008D4	00000000			498		DC	A(0)
000008D8	00000000			499		DC	A(0)
							end of table end of table
				501			PRINT NODATA

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				503 *****
				504 * TRTR op1 scan data...
				505 *****
000008DC	78125634 78125634			507 TRTOP10 DC 64XL4'78125634' (CC0)
000009DC	00F00000 78125634			509 TRTOP1F0 DC X'00F00000',63XL4'78125634' (CC1)
00000ADC	F1000000 78125634			511 TRTOP1F1 DC X'F1000000',63XL4'78125634' (CC2)
				513 *****
				514 * Function Code (FC) Tables
				515 *****
00000BDC	00000000 00000000			517 TRTOP20 DC 256X'00' no stop
00000CE0	00000000 00000000			518 DS D
00000CE8	00000000 00000000			520 TRTOP2F0 DC 240X'00',X'F0',15X'00' stop on X'F0'
00000DE8	00000000 00000000			521 DS D
00000DF0	00000000 00000000			523 TRTOP8F1 DC 240X'00',X'00',X'F1',14X'00' stop on X'F1'
00000EF0	00000000 00000000			524 DS D
				526 *****
				527 * Register equates
				528 *****
	00000000	00000001		530 R0 EQU 0
	00000001	00000001		531 R1 EQU 1
	00000002	00000001		532 R2 EQU 2
	00000003	00000001		533 R3 EQU 3
	00000004	00000001		534 R4 EQU 4
	00000005	00000001		535 R5 EQU 5
	00000006	00000001		536 R6 EQU 6
	00000007	00000001		537 R7 EQU 7
	00000008	00000001		538 R8 EQU 8
	00000009	00000001		539 R9 EQU 9
	0000000A	00000001		540 R10 EQU 10
	0000000B	00000001		541 R11 EQU 11
	0000000C	00000001		542 R12 EQU 12
	0000000D	00000001		543 R13 EQU 13
	0000000E	00000001		544 R14 EQU 14
	0000000F	00000001		545 R15 EQU 15

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				547
				END

MACRO DEFN REFERENCES

No defined macros

DESC	SYMBOL	SIZE	POS	ADDR
------	--------	------	-----	------

Entry: 0

Image	IMAGE	3832	000-EF7	000-EF7
Region		3832	000-EF7	000-EF7
CSECT	TRTR1TST	3832	000-EF7	000-EF7

STMT FILE NAME

1 /devstor/dev/tests/TRTR-01-basic.asm

** NO ERRORS FOUND **