```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                     2 ************************************************************************
                                                     3 *
                                                     4 *   Zvector E7 instruction tests for VRR-a encoded:
                                                     5 *
                                                     6 *   E750 VPOPCT - Vector Population Count
                                                     7 *   E752 VCTZ   - Vector Count Trailing Zeros
                                                     8 *   E753 VCLZ   - Vector Count Leading Zeros
                                                     9 *
                                                    10 *        James Wekel January 2025
                                                    11 ************************************************************************

                                                    13 ************************************************************************
                                                    14 *
                                                    15 *        basic instruction tests
                                                    16 *
                                                    17 ************************************************************************
                                                    18 *  This program tests proper functioning of the z/arch E7 VRR-a
                                                    19 *  bit count instructions: Vector Population Count, Vector Count
                                                    20 *  Trailing Zeros, and Vector Count Leading Zeros.
                                                    21 *  Exceptions are not tested.
                                                    22 *
                                                    23 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                    24 *  obvious coding errors.  None of the tests are thorough.  They are
                                                    25 *  NOT designed to test all aspects of any of the instructions.
                                                    26 *
                                                    27 ************************************************************************
                                                    28 *
                                                    29 *   *Testcase zvector-e7-04-BitCount
                                                    30 *   *
                                                    31 *   *   Zvector E7 instruction tests for VRR-a encoded:
                                                    32 *   *
                                                    33 *   *   E750 VPOPCT - Vector Population Count
                                                    34 *   *   E752 VCTZ   - Vector Count Trailing Zeros
                                                    35 *   *   E753 VCLZ   - Vector Count Leading Zeros
                                                    36 *   *
                                                    37 *   *   # ------------------------------------------------------------
                                                    38 *   *   #  This tests only the basic function of the instruction.
                                                    39 *   *   #  Exceptions are NOT tested.
                                                    40 *   *   # ------------------------------------------------------------
                                                    41 *   *
                                                    42 *   mainsize    2
                                                    43 *   numcpu      1
                                                    44 *   sysclear
                                                    45 *   archlvl     z/Arch
                                                    46 *
                                                    47 *   loadcore    "$(testpath)/zvector-e7-04-BitCount.core" 0x0
                                                    48 *
                                                    49 *   diag8cmd    enable    # (needed for messages to Hercules console)
                                                    50 *   runtest     10        # (2 secs if intrinsic used, 10 otherwise!)
                                                    51 *   diag8cmd    disable   # (reset back to default)
                                                    52 *
                                                    53 *   *Done
                                                    54 *
                                                    55 *
                                                    56 ************************************************************************
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    58 ************************************************************************
                                                    59 *        FCHECK Macro - Is a Facility Bit set?
                                                    60 *
                                                    61 *        If the facility bit is NOT set, an message is issued and
                                                    62 *        the test is skipped.
                                                    63 *
                                                    64 *        Fcheck uses R0, R1 and R2
                                                    65 *
                                                    66 * eg.    FCHECK 134,'vector-packed-decimal'
                                                    67 ************************************************************************
                                                    68          MACRO
                                                    69          FCHECK &BITNO,&NOTSETMSG
                                                    70 .*                      &BITNO : facility bit number to check
                                                    71 .*                      &NOTSETMSG : 'facility name'
                                                    72          LCLA  &FBBYTE           Facility bit in Byte
                                                    73          LCLA  &FBBIT            Facility bit within Byte
                                                    74
                                                    75          LCLA  &L(8)
                                                    76 &L(1)    SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                                    77
                                                    78 &FBBYTE  SETA  &BITNO/8
                                                    79 &FBBIT   SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                                    80 .*       MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                                    81
                                                    82          B     X&SYSNDX
                                                    83 *                                       Fcheck data area
                                                    84 *                                       skip messgae
                                                    85 SKT&SYSNDX DC  C'    Skipping tests: '
                                                    86          DC    C&NOTSETMSG
                                                    87          DC    C' (bit &BITNO) is not installed.'
                                                    88 SKL&SYSNDX EQU *-SKT&SYSNDX
                                                    89 *                                       facility bits
                                                    90          DS    FD                       gap
                                                    91 FB&SYSNDX DS   4FD
                                                    92          DS    FD                       gap
                                                    93 *
                                                    94 X&SYSNDX EQU *
                                                    95          LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                                    96          STFLE FB&SYSNDX                get facility bits
                                                    97
                                                    98          XGR   R0,R0
                                                    99          IC    R0,FB&SYSNDX+&FBBYTE     get fbit byte
                                                   100          N     R0,=F'&FBBIT'            is bit set?
                                                   101          BNZ   XC&SYSNDX
                                                   102 *
                                                   103 * facility bit not set, issue message and exit
                                                   104 *
                                                   105          LA    R0,SKL&SYSNDX            message length
                                                   106          LA    R1,SKT&SYSNDX            message address
                                                   107          BAL   R2,MSG
                                                   108
                                                   109          B     EOJ
                                                   110 XC&SYSNDX EQU *
                                                   111          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     113 ************************************************************************
                                                     114 *        Low core PSWs
                                                     115 ************************************************************************
                               00000000  00002B17    116 ZVE7TST  START 0
00000000                       00000000              117          USING ZVE7TST,R0            Low core addressability
                                                     118
                               00000140  00000000    119 SVOLDPSW EQU   ZVE7TST+X'140'        z/Arch Supervisor call old PSW

00000000                       00000000  000001A0    121          ORG   ZVE7TST+X'1A0'        z/Architecure RESTART PSW
000001A0  00000001 80000000                          122          DC    X'0000000180000000'
000001A8  00000000 00000200                          123          DC    AD(BEGIN)

000001B0                       000001B0  000001D0    125          ORG   ZVE7TST+X'1D0'        z/Architecure PROGRAM CHECK PSW
000001D0  00020001 80000000                          126          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                          127          DC    AD(X'DEAD')

000001E0                       000001E0  00000200    129          ORG   ZVE7TST+X'200'        Start of actual test program...

                                                     131 ************************************************************************
                                                     132 *                The actual "ZVE7TST" program itself...
                                                     133 ************************************************************************
                                                     134 *
                                                     135 *  Architecture Mode: z/Arch
                                                     136 *  Register Usage:
                                                     137 *
                                                     138 *    R0       (work)
                                                     139 *    R1-4     (work)
                                                     140 *    R5       Testing control table - current test base
                                                     141 *    R6-R7    (work)
                                                     142 *    R8       First base register
                                                     143 *    R9       Second base register
                                                     144 *    R10      Third base register
                                                     145 *    R11      E7TEST call return
                                                     146 *    R12      E7TESTS register
                                                     147 *    R13      (work)
                                                     148 *    R14      Subroutine call
                                                     149 *    R15      Secondary Subroutine call or work
                                                     150 *
                                                     151 ************************************************************************

00000200                       00000200              153          USING BEGIN,R8          FIRST Base Register
00000200                       00001200              154          USING BEGIN+4096,R9     SECOND Base Register
00000200                       00002200              155          USING BEGIN+8192,R10    THIRD Base Register

00000200  0580                                       157 BEGIN    BALR  R8,0              Initalize FIRST base register
00000202  0680                                       158          BCTR  R8,0              Initalize FIRST base register
00000204  0680                                       159          BCTR  R8,0              Initalize FIRST base register

00000206  4190 8800                    00000800      161          LA    R9,2048(,R8)      Initalize SECOND base register
0000020A  4190 9800                    00000800      162          LA    R9,2048(,R9)      Initalize SECOND base register
                                                     163
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
0000020E  41A0 9800                    00000800   164          LA    R10,2048(,R9)    Initalize THIRD base register
00000212  41A0 A800                    00000800   165          LA    R10,2048(,R10)   Initalize THIRD base register
                                                  166
00000216  B600 828C                    0000048C   167          STCTL R0,R0,CTLR0      Store CR0 to enable AFP
0000021A  9604 828D                    0000048D   168          OI    CTLR0+1,X'04'    Turn on AFP bit
0000021E  9602 828D                    0000048D   169          OI    CTLR0+1,X'02'    Turn on Vector bit
00000222  B700 828C                    0000048C   170          LCTL  R0,R0,CTLR0      Reload updated CR0
                                                  171
                                                  172 ********************************************************************
                                                  173 * Is z/Architecture vector facility installed  (bit 129)
                                                  174 ********************************************************************
                                                  175
                                                  176          FCHECK 129,'z/Architecture vector facility'
00000226  47F0 80A8                    000002A8  177+         B     X0001
                                                  178+*                                  Fcheck data area
                                                  179+*                                  skip messgae
0000022A  40404040 E2928997                       180+SKT0001  DC    C'    Skipping tests: '
0000023E  A961C199 838889A3                       181+         DC    C'z/Architecture vector facility'
0000025C  404D8289 A340F1F2                       182+         DC    C' (bit 129) is not installed.'
                           0000004E  00000001     183+SKL0001  EQU   *-SKT0001
                                                  184+*                                  facility bits
00000278  00000000 00000000                       185+         DS    FD                 gap
00000280  00000000 00000000                       186+FB0001   DS    4FD
000002A0  00000000 00000000                       187+         DS    FD                 gap
                                                  188+*
                           000002A8  00000001     189+X0001    EQU   *
000002A8  4100 0004                    00000004   190+         LA    R0,((X0001-FB0001)/8)-1
000002AC  B2B0 8080                    00000280   191+         STFLE FB0001             get facility bits
000002B0  B982 0000                               192+         XGR   R0,R0
000002B4  4300 8090                    00000290   193+         IC    R0,FB0001+16       get fbit byte
000002B8  5400 8294                    00000494   194+         N     R0,=F'64'          is bit set?
000002BC  4770 80D0                    000002D0   195+         BNZ   XC0001
                                                  196+*
                                                  197+* facility bit not set, issue message and exit
                                                  198+*
000002C0  4100 004E                    0000004E   199+         LA    R0,SKL0001         message length
000002C4  4110 802A                    0000022A   200+         LA    R1,SKT0001         message address
000002C8  4520 81A8                    000003A8   201+         BAL   R2,MSG
000002CC  47F0 8270                    00000470   202+         B     EOJ
                           000002D0  00000001     203+XC0001   EQU   *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    205 ************************************************************************
                                                    206 *               Do tests in the E7TESTS table
                                                    207 ************************************************************************
                                                    208
000002D0  58C0 8298                       00000498 209          L     R12,=A(E7TESTS)          get table of test addresses
                                                    210
                                 000002D4  00000001 211 NEXTE7   EQU   *
000002D4  5850 C000                       00000000 212          L     R5,0(0,R12)              get test address
000002D8  1255                                     213          LTR   R5,R5                       have a test?
000002DA  4780 811E                       0000031E 214          BZ    ENDTEST                        done?
                                                    215
000002DE                          00000000         216          USING E7TEST,R5
                                                    217
000002DE  4800 5004                       00000004 218          LH    R0,TNUM                  save current test number
000002E2  5000 8E04                       00001004 219          ST    R0,TESTING               for easy reference
                                                    220
000002E6  E710 8E94 0006                  00001094 221          VL    V1,V1FUDGE
000002EC  58B0 5000                       00000000 222          L     R11,TSUB                 get address of test routine
000002F0  05BB                                     223          BALR  R11,R11                  do test
                                                    224
000002F2  E310 5018 0014                  00000018 225          LGF   R1,READDR                get address of expected result
000002F8  D50F 5028 1000        00000028  00000000 226          CLC   V1OUTPUT,0(R1)           valid?
000002FE  4770 810A                       0000030A 227          BNE   FAILMSG                     no, issue failed message
                                                    228
00000302  41C0 C004                       00000004 229          LA    R12,4(0,R12)             next test address
00000306  47F0 80D4                       000002D4 230          B     NEXTE7
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    232 ************************************************************************
                                                    233 * result not as expected:
                                                    234 *        issue message with test number, instruction under test
                                                    235 *              and instruction m4
                                                    236 ************************************************************************
                             0000030A  00000001     237 FAILMSG  EQU   *
0000030A  45F0 812C                    0000032C     238          BAL   R15,RPTERROR

                                                    240 ************************************************************************
                                                    241 * continue after a failed test
                                                    242 ************************************************************************
                             0000030E  00000001     243 FAILCONT EQU   *
0000030E  5800 829C                    0000049C     244          L     R0,=F'1'                set failed test indicator
00000312  5000 8E00                    00001000     245          ST    R0,FAILED
                                                    246
00000316  41C0 C004                    00000004     247          LA    R12,4(0,R12)            next test address
0000031A  47F0 80D4                    000002D4     248          B     NEXTE7


                                                    250 ************************************************************************
                                                    251 * end of testing; set ending psw
                                                    252 ************************************************************************
                             0000031E  00000001     253 ENDTEST  EQU   *
0000031E  5810 8E00                    00001000     254          L     R1,FAILED               did a test fail?
00000322  1211                                      255          LTR   R1,R1
00000324  4780 8270                    00000470     256          BZ    EOJ                     No, exit
00000328  47F0 8288                    00000488     257          B     FAILTEST                Yes, exit with BAD PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   259 ********************************************************************************
                                                   260 *        RPTERROR                  Report instruction test in error
                                                   261 ********************************************************************************

0000032C  50F0 8190                        00000390   263 RPTERROR ST    R15,RPTSAVE             Save return address
00000330  5050 8194                        00000394   264          ST    R5,RPTSVR5              Save R5
                                                   265 *
00000334  4820 5004                        00000004   266          LH    R2,TNUM                 get test number and convert
00000338  4E20 8E73                        00001073   267          CVD   R2,DECNUM
0000033C  D211 8E5D 8E47       0000105D    00001047   268          MVC   PRT3,EDIT
00000342  DE11 8E5D 8E73       0000105D    00001073   269          ED    PRT3,DECNUM
00000348  D202 8E18 8E6A       00001018    0000106A   270          MVC   PRTNUM(3),PRT3+13       fill in message with test #
                                                   271
0000034E  D207 8E33 5008       00001033    00000008   272          MVC   PRTNAME,OPNAME          fill in message with instruction
                                                   273 *
00000354  E320 5007 0076                   00000007   274          LB    R2,M3                   get M3 and convert
0000035A  4E20 8E73                        00001073   275          CVD   R2,DECNUM
0000035E  D211 8E5D 8E47       0000105D    00001047   276          MVC   PRT3,EDIT
00000364  DE11 8E5D 8E73       0000105D    00001073   277          ED    PRT3,DECNUM
0000036A  D201 8E44 8E6B       00001044    0000106B   278          MVC   PRTM3(2),PRT3+14        fill in message with m3 field

                                                   280 *
                                                   281 *        Use Hercules Diagnose for Message to console
                                                   282 *
00000370  9002 8198                        00000398   283          STM   R0,R2,RPTDWSAV          save regs used by MSG
00000374  4100 003F                        0000003F   284          LA    R0,PRTLNG               message length
00000378  4110 8E08                        00001008   285          LA    R1,PRTLINE              messagfe address
0000037C  4520 81A8                        000003A8   286          BAL   R2,MSG                  call Hercules to display MSG
00000380  9802 8198                        00000398   287          LM    R0,R2,RPTDWSAV          restore regs


00000384  5850 8194                        00000394   289          L     R5,RPTSVR5              Restore R5
00000388  58F0 8190                        00000390   290          L     R15,RPTSAVE             Restore return address
0000038C  07FF                                     291          BR    R15                     Return to caller

00000390  00000000                                 293 RPTSAVE  DC    F'0'                    R15 save area
00000394  00000000                                 294 RPTSVR5  DC    F'0'                    R5 save area

00000398  00000000 00000000                        296 RPTDWSAV DC    2D'0'                   R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    298 ************************************************************************
                                                    299 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                    300 *              R2 = return address
                                                    301 ************************************************************************
000003A8  4900 82A0                      000004A0   303 MSG      CH    R0,=H'0'                Do we even HAVE a message?
000003AC  07D2                                      304          BNHR  R2                      No, ignore

000003AE  9002 81E4                      000003E4   306          STM   R0,R2,MSGSAVE            Save registers

000003B2  4900 82A2                      000004A2   308          CH    R0,=AL2(L'MSGMSG)       Message length within limits?
000003B6  47D0 81BE                      000003BE   309          BNH   MSGOK                   Yes, continue
000003BA  4100 005F                      0000005F   310          LA    R0,L'MSGMSG             No, set to maximum

000003BE  1820                                      312 MSGOK    LR    R2,R0                   Copy length to work register
000003C0  0620                                      313          BCTR  R2,0                    Minus-1 for execute
000003C2  4420 81F0                      000003F0   314          EX    R2,MSGMVC               Copy message to O/P buffer

000003C6  4120 200A                      0000000A   316          LA    R2,1+L'MSGCMD(,R2)      Calculate true command length
000003CA  4110 81F6                      000003F6   317          LA    R1,MSGCMD               Point to true command

000003CE  83120008                                  319          DC    X'83',X'12',X'0008'     Issue Hercules Diagnose X'008'
000003D2  4780 81DE                      000003DE   320          BZ    MSGRET                  Return if successful
                                                    321
000003D6  1222                                      322          LTR   R2,R2                   Is Diag8 Ry (R2) 0?
000003D8  4780 81DE                      000003DE   323          BZ    MSGRET                    an error occurred but coninue
                                                    324
000003DC  0000                                      325          DC    H'0'                    CRASH for debugging purposes

000003DE  9802 81E4                      000003E4   327 MSGRET   LM    R0,R2,MSGSAVE           Restore registers
000003E2  07F2                                      328          BR    R2                      Return to caller

000003E4  00000000 00000000                         330 MSGSAVE  DC    3F'0'                   Registers save area
000003F0  D200 81FF 1000      000003FF  00000000    331 MSGMVC   MVC   MSGMSG(0),0(R1)          Executed instruction

000003F6  D4E2C7D5 D6C8405C                         333 MSGCMD   DC    C'MSGNOH * '            *** HERCULES MESSAGE COMMAND ***
000003FF  40404040 40404040                         334 MSGMSG   DC    CL95' '                 The message text to be displayed
                                                    335
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                     337 ************************************************************************
                                                     338 *        Normal completion or Abnormal termination PSWs
                                                     339 ************************************************************************

00000460  00020001 80000000                          341 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)
00000470  B2B2 8260                    00000460      343 EOJ      LPSWE EOJPSW                   Normal completion

00000478  00020001 80000000                          345 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')
00000488  B2B2 8278                    00000478      347 FAILTEST LPSWE FAILPSW                  Abnormal termination

                                                     349 ************************************************************************
                                                     350 *        Working Storage
                                                     351 ************************************************************************

0000048C  00000000                                   353 CTLR0    DS    F                        CR0
00000490  00000000                                   354          DS    F

00000494                                             356          LTORG ,                        Literals pool
00000494  00000040                                   357                =F'64'
00000498  00002A3C                                   358                =A(E7TESTS)
0000049C  00000001                                   359                =F'1'
000004A0  0000                                       360                =H'0'
000004A2  005F                                       361                =AL2(L'MSGMSG)
                                                     362
                                                     363 *        some constants
                                                     364
                          00000400  00000001         365 K        EQU   1024                     One KB
                          00001000  00000001         366 PAGE     EQU   (4*K)                    Size of one page
                          00010000  00000001         367 K64      EQU   (64*K)                   64 KB
                          00100000  00000001         368 MB       EQU   (K*K)                     1 MB
                                                     369
                          AABBCCDD  00000001         370 REG2PATT EQU   X'AABBCCDD'              Polluted Register pattern
                          000000DD  00000001         371 REG2LOW  EQU         X'DD'             (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     373 *=========================================================================
                                                     374 *
                                                     375 *  NOTE: start data on an address that is easy to display
                                                     376 *        within Hercules
                                                     377 *
                                                     378 *=========================================================================
                                                     379
000004A4                      000004A4  00001000     380          ORG   ZVE7TST+X'1000'
00001000  00000000                                   381 FAILED   DC    F'0'                    some test failed?
00001004  00000000                                   382 TESTING  DC    F'0'                    current test number

                                                     384 *
                                                     385 *        failed message and associated editting
                                                     386 *
00001008  40404040 40404040                          387 PRTLINE  DC    C'         Test # '
00001018  A7A7A7                                     388 PRTNUM   DC    C'xxx'
0000101B  40868189 93858440                          389          DC    c' failed for instruction '
00001033  A7A7A7A7 A7A7A7A7                          390 PRTNAME  DC    CL8'xxxxxxxx'
0000103B  40A689A3 8840D4F3                          391          DC    C' with M3='
00001044  A7A7                                       392 PRTM3    DC    C'xx'
00001046  4B                                         393          DC    C'.'
                                0000003F  00000001   394 PRTLNG   EQU   *-PRTLINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    396 ************************************************************************
                                                    397 *        TEST failed : message working storge
                                                    398 ************************************************************************
00001047  40212020 20202020                         399 EDIT     DC    XL18'40212020202020202020202020202020'
                                                    400
00001059  7E7E7E6E                                  401          DC    C'===>'
0000105D  40404040 40404040                         402 PRT3     DC    CL18' '
0000106F  4C7E7E7E                                  403          DC    C'<==='
00001073  00000000 00000000                         404 DECNUM   DS    CL16


                                                    406 ************************************************************************
                                                    407 *        Vector instruction results, pollution and input
                                                    408 ************************************************************************
00001084                                            409          DS    0F
00001084  00000000 00000000                         410          DS    XL16                                        gap
00001094  FFFFFFFF FFFFFFFF                         411 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
000010A4  00000000 00000000                         412          DS    XL16
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    414 ********************************************************************************
                                                    415 *        E7TEST DSECT
                                                    416 ********************************************************************************


                                                    418 E7TEST   DSECT ,
00000000  00000000                                  419 TSUB     DC    A(0)                    pointer  to test
00000004  0000                                      420 TNUM     DC    H'00'                   Test Number
00000006  00                                        421          DC    X'00'
00000007  00                                        422 M3       DC    HL1'00'                 m4 used
                                                    423
00000008  40404040 40404040                         424 OPNAME   DC    CL8' '                  E6 name
00000010  00000000                                  425 V2ADDR   DC    A(0)                    address of v2 source
00000014  00000000                                  426 RELEN    DC    A(0)                    RESULT LENGTH
00000018  00000000                                  427 READDR   DC    A(0)                    result (expected) address
00000020  00000000 00000000                         428          DS    FD                         gap
00000028  00000000 00000000                         429 V1OUTPUT DS    XL16                    V1 Output
00000038  00000000 00000000                         430          DS    FD                         gap
                                                    431
                                                    432 *        test routine will be here (from VRR-a macro)
                                                    433 *
                                                    434 *        followed by
                                                    435 *              EXPECTED RESULT


                          00000000  00002B17        437 ZVE7TST  CSECT ,
000010B4                                            438          DS    0F


                                                    440 ********************************************************************************
                                                    441 *     Macros to help build test tables
                                                    442 ********************************************************************************


                                                    444 *
                                                    445 * macro to generate individual test
                                                    446 *
                                                    447          MACRO
                                                    448          VRR_A &INST,&M3
                                                    449 .*                                &INST   - VRR-a instruction under test
                                                    450 .*                                &M3     - m3 field
                                                    451
                                                    452          GBLA  &TNUM
                                                    453 &TNUM    SETA  &TNUM+1
                                                    454
                                                    455          DS    0FD
                                                    456          USING *,R5                base for test data and test routine
                                                    457
                                                    458 T&TNUM   DC    A(X&TNUM)           address of test routine
                                                    459          DC    H'&TNUM'            test number
                                                    460          DC    X'00'
                                                    461          DC    HL1'&M3'            M3
                                                    462          DC    CL8'&INST'          instruction name
                                                    463          DC    A(RE&TNUM+16)       address of v2 source
                                                    464          DC    A(16)               result length
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                      465 REA&TNUM DC    A(RE&TNUM)          result address
                                                      466          DS    FD                  gap
                                                      467 V1O&TNUM DS    XL16                V1 output
                                                      468          DS    FD                  gap
                                                      469 .*
                                                      470 *
                                                      471 X&TNUM   DS    0F
                                                      472          LGF   R1,V2ADDR           load v2 source
                                                      473          VL    v22,0(R1)           use v22 to test decoder
                                                      474
                                                      475          &INST V22,V22,&M3         test instruction (dest is a source)
                                                      476          VST   V22,V1O&TNUM        save v1 output
                                                      477
                                                      478          BR    R11                 return
                                                      479
                                                      480 RE&TNUM  DC    0F                  xl16 expected result
                                                      481
                                                      482          DROP  R5
                                                      483          MEND



                                                      485 *
                                                      486 * macro to generate table of pointers to individual tests
                                                      487 *
                                                      488          MACRO
                                                      489          PTTABLE
                                                      490          GBLA  &TNUM
                                                      491          LCLA  &CUR
                                                      492 &CUR     SETA  1
                                                      493 .*
                                                      494 TTABLE   DS    0F
                                                      495 .LOOP    ANOP
                                                      496 .*
                                                      497          DC    A(T&CUR)            TEST &CUR
                                                      498 .*
                                                      499 &CUR     SETA  &CUR+1
                                                      500          AIF   (&CUR LE &TNUM).LOOP
                                                      501 *
                                                      502          DC    A(0)                END OF TABLE
                                                      503          DC    A(0)                END OF TABLE
                                                      504 .*
                                                      505          MEND
                                                      506
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   508 ************************************************************************
                                                   509 *        E7 VRR-a tests
                                                   510 ************************************************************************
                                                   511          PRINT DATA
                                                   512 *
                                                   513 *   E750 VPOPCT - Vector Population Count
                                                   514 *   E752 VCTZ   - Vector Count Trailing Zeros
                                                   515 *   E753 VCLZ   - Vector Count Leading Zeros
                                                   516 *
                                                   517 *        VRR-a instruction, M3
                                                   518 *             followed by
                                                   519 *                16 byte expected result (V1)
                                                   520 *                16 byte V2 source
                                                   521 *-----------------------------------------------------------------
                                                   522 * VPOPCT - Vector Population Count
                                                   523 *-----------------------------------------------------------------
                                                   524
                                                   525 *-----------------------------------------------------------------
                                                   526 * case 0 - simple, simple debug
                                                   527 *-----------------------------------------------------------------
                                                   528 * Byte
                                                   529          VRR_A VPOPCT,0
000010B8                                           530+         DS    0FD
000010B8                          000010B8         531+         USING *,R5              base for test data and test routine
000010B8  000010F8                                 532+T1       DC    A(X1)             address of test routine
000010BC  0001                                     533+         DC    H'1'              test number
000010BE  00                                       534+         DC    X'00'
000010BF  00                                       535+         DC    HL1'0'            M3
000010C0  E5D7D6D7 C3E34040                        536+         DC    CL8'VPOPCT'       instruction name
000010C8  00001124                                 537+         DC    A(RE1+16)         address of v2 source
000010CC  00000010                                 538+         DC    A(16)             result length
000010D0  00001114                                 539+REA1     DC    A(RE1)            result address
000010D8  00000000 00000000                        540+         DS    FD                gap
000010E0  00000000 00000000                        541+V1O1     DS    XL16              V1 output
000010E8  00000000 00000000
000010F0  00000000 00000000                        542+         DS    FD                gap
                                                   543+*
000010F8                                           544+X1       DS    0F
000010F8  E310 5010 0014                 00000010  545+         LGF   R1,V2ADDR         load v2 source
000010FE  E761 0000 0806                 00000000  546+         VL    v22,0(R1)         use v22 to test decoder
00001104  E766 0000 0C50                           547+         VPOPCT V22,V22,0        test instruction (dest is a source)
0000110A  E760 5028 080E                 000010E0  548+         VST   V22,V1O1          save v1 output
00001110  07FB                                     549+         BR    R11               return
00001114                                           550+RE1      DC    0F                xl16 expected result
00001114                                           551+         DROP  R5
00001114  00000000 00000000                        552          DC    XL16'00000000000000000000000000000000'   expected result
0000111C  00000000 00000000
00001124  00000000 00000000                        553          DC    XL16'00000000000000000000000000000000'   v2
0000112C  00000000 00000000
                                                   554
                                                   555 * Halfword
                                                   556          VRR_A VPOPCT,1
00001138                                           557+         DS    0FD
00001138                          00001138         558+         USING *,R5              base for test data and test routine
00001138  00001178                                 559+T2       DC    A(X2)             address of test routine
0000113C  0002                                     560+         DC    H'2'              test number
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
0000113E  00                                       561+         DC    X'00'
0000113F  01                                       562+         DC    HL1'1'              M3
00001140  E5D7D6D7 C3E34040                        563+         DC    CL8'VPOPCT'         instruction name
00001148  000011A4                                 564+         DC    A(RE2+16)           address of v2 source
0000114C  00000010                                 565+         DC    A(16)               result length
00001150  00001194                                 566+REA2     DC    A(RE2)              result address
00001158  00000000 00000000                        567+         DS    FD                  gap
00001160  00000000 00000000                        568+V1O2     DS    XL16                V1 output
00001168  00000000 00000000
00001170  00000000 00000000                        569+         DS    FD                  gap
                                                   570+*
00001178                                           571+X2       DS    0F
00001178  E310 5010 0014                 00000010  572+         LGF   R1,V2ADDR           load v2 source
0000117E  E761 0000 0806                 00000000  573+         VL    v22,0(R1)           use v22 to test decoder
00001184  E766 0000 1C50                           574+         VPOPCT V22,V22,1          test instruction (dest is a source)
0000118A  E760 5028 080E                 00001160  575+         VST   V22,V1O2            save v1 output
00001190  07FB                                     576+         BR    R11                 return
00001194                                           577+RE2      DC    0F                  xl16 expected result
00001194                                           578+         DROP  R5
00001194  00000000 00000000                        579          DC    XL16'00000000000000000000000000000000'   expected result
0000119C  00000000 00000000
000011A4  00000000 00000000                        580          DC    XL16'00000000000000000000000000000000'   v2
000011AC  00000000 00000000
                                                   581
                                                   582 * Word
                                                   583          VRR_A VPOPCT,2
000011B8                                           584+         DS    0FD
000011B8                      000011B8             585+         USING *,R5                base for test data and test routine
000011B8  000011F8                                 586+T3       DC    A(X3)               address of test routine
000011BC  0003                                     587+         DC    H'3'                test number
000011BE  00                                       588+         DC    X'00'
000011BF  02                                       589+         DC    HL1'2'              M3
000011C0  E5D7D6D7 C3E34040                        590+         DC    CL8'VPOPCT'         instruction name
000011C8  00001224                                 591+         DC    A(RE3+16)           address of v2 source
000011CC  00000010                                 592+         DC    A(16)               result length
000011D0  00001214                                 593+REA3     DC    A(RE3)              result address
000011D8  00000000 00000000                        594+         DS    FD                  gap
000011E0  00000000 00000000                        595+V1O3     DS    XL16                V1 output
000011E8  00000000 00000000
000011F0  00000000 00000000                        596+         DS    FD                  gap
                                                   597+*
000011F8                                           598+X3       DS    0F
000011F8  E310 5010 0014                 00000010  599+         LGF   R1,V2ADDR           load v2 source
000011FE  E761 0000 0806                 00000000  600+         VL    v22,0(R1)           use v22 to test decoder
00001204  E766 0000 2C50                           601+         VPOPCT V22,V22,2          test instruction (dest is a source)
0000120A  E760 5028 080E                 000011E0  602+         VST   V22,V1O3            save v1 output
00001210  07FB                                     603+         BR    R11                 return
00001214                                           604+RE3      DC    0F                  xl16 expected result
00001214                                           605+         DROP  R5
00001214  00000000 00000000                        606          DC    XL16'00000000000000000000000000000000'   expected result
0000121C  00000000 00000000
00001224  00000000 00000000                        607          DC    XL16'00000000000000000000000000000000'   v2
0000122C  00000000 00000000
                                                   608
                                                   609 * Doubleword
                                                   610          VRR_A VPOPCT,3
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001238                                           611+         DS    0FD
00001238                       00001238            612+         USING *,R5               base for test data and test routine
00001238  00001278                                 613+T4       DC    A(X4)              address of test routine
0000123C  0004                                     614+         DC    H'4'               test number
0000123E  00                                       615+         DC    X'00'
0000123F  03                                       616+         DC    HL1'3'             M3
00001240  E5D7D6D7 C3E34040                        617+         DC    CL8'VPOPCT'        instruction name
00001248  000012A4                                 618+         DC    A(RE4+16)          address of v2 source
0000124C  00000010                                 619+         DC    A(16)              result length
00001250  00001294                                 620+REA4     DC    A(RE4)             result address
00001258  00000000 00000000                        621+         DS    FD                 gap
00001260  00000000 00000000                        622+V1O4     DS    XL16               V1 output
00001268  00000000 00000000
00001270  00000000 00000000                        623+         DS    FD                 gap
                                                   624+*
00001278                                           625+X4       DS    0F
00001278  E310 5010 0014                 00000010  626+         LGF   R1,V2ADDR          load v2 source
0000127E  E761 0000 0806                 00000000  627+         VL    v22,0(R1)          use v22 to test decoder
00001284  E766 0000 3C50                           628+         VPOPCT V22,V22,3         test instruction (dest is a source)
0000128A  E760 5028 080E                 00001260  629+         VST   V22,V1O4           save v1 output
00001290  07FB                                     630+         BR    R11                return
00001294                                           631+RE4      DC    0F                 xl16 expected result
00001294                                           632+         DROP  R5
00001294  00000000 00000000                        633          DC    XL16'00000000000000000000000000000000'   expected result
0000129C  00000000 00000000
000012A4  00000000 00000000                        634          DC    XL16'00000000000000000000000000000000'   v2
000012AC  00000000 00000000
                                                   635
                                                   636 *-------------------------------------------------------------------
                                                   637 * Byte
                                                   638          VRR_A VPOPCT,0
000012B8                                           639+         DS    0FD
000012B8                       000012B8            640+         USING *,R5               base for test data and test routine
000012B8  000012F8                                 641+T5       DC    A(X5)              address of test routine
000012BC  0005                                     642+         DC    H'5'               test number
000012BE  00                                       643+         DC    X'00'
000012BF  00                                       644+         DC    HL1'0'             M3
000012C0  E5D7D6D7 C3E34040                        645+         DC    CL8'VPOPCT'        instruction name
000012C8  00001324                                 646+         DC    A(RE5+16)          address of v2 source
000012CC  00000010                                 647+         DC    A(16)              result length
000012D0  00001314                                 648+REA5     DC    A(RE5)             result address
000012D8  00000000 00000000                        649+         DS    FD                 gap
000012E0  00000000 00000000                        650+V1O5     DS    XL16               V1 output
000012E8  00000000 00000000
000012F0  00000000 00000000                        651+         DS    FD                 gap
                                                   652+*
000012F8                                           653+X5       DS    0F
000012F8  E310 5010 0014                 00000010  654+         LGF   R1,V2ADDR          load v2 source
000012FE  E761 0000 0806                 00000000  655+         VL    v22,0(R1)          use v22 to test decoder
00001304  E766 0000 0C50                           656+         VPOPCT V22,V22,0         test instruction (dest is a source)
0000130A  E760 5028 080E                 000012E0  657+         VST   V22,V1O5           save v1 output
00001310  07FB                                     658+         BR    R11                return
00001314                                           659+RE5      DC    0F                 xl16 expected result
00001314                                           660+         DROP  R5
00001314  08080808 08080808                        661          DC    XL16'08080808080808080808080808080808'   expected result
0000131C  08080808 08080808
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001324  FFFFFFFF FFFFFFFF                          662          DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'   v2
0000132C  FFFFFFFF FFFFFFFF
                                                    663
                                                    664 * Halfword
                                                    665          VRR_A VPOPCT,1
00001338                                            666+         DS    0FD
00001338                      00001338              667+         USING *,R5               base for test data and test routine
00001338  00001378                                  668+T6       DC    A(X6)              address of test routine
0000133C  0006                                      669+         DC    H'6'               test number
0000133E  00                                        670+         DC    X'00'
0000133F  01                                        671+         DC    HL1'1'             M3
00001340  E5D7D6D7 C3E34040                         672+         DC    CL8'VPOPCT'        instruction name
00001348  000013A4                                  673+         DC    A(RE6+16)          address of v2 source
0000134C  00000010                                  674+         DC    A(16)              result length
00001350  00001394                                  675+REA6     DC    A(RE6)             result address
00001358  00000000 00000000                         676+         DS    FD                 gap
00001360  00000000 00000000                         677+V1O6     DS    XL16               V1 output
00001368  00000000 00000000
00001370  00000000 00000000                         678+         DS    FD                 gap
                                                    679+*
00001378                                            680+X6       DS    0F
00001378  E310 5010 0014                 00000010   681+         LGF   R1,V2ADDR          load v2 source
0000137E  E761 0000 0806                 00000000   682+         VL    v22,0(R1)          use v22 to test decoder
00001384  E766 0000 1C50                            683+         VPOPCT V22,V22,1         test instruction (dest is a source)
0000138A  E760 5028 080E                 00001360   684+         VST   V22,V1O6           save v1 output
00001390  07FB                                      685+         BR    R11                return
00001394                                            686+RE6      DC    0F                 xl16 expected result
00001394                                            687+         DROP  R5
00001394  00100010 00100010                         688          DC    XL16'00100010001000100010001000100010'   expected result
0000139C  00100010 00100010
000013A4  FFFFFFFF FFFFFFFF                         689          DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'   v2
000013AC  FFFFFFFF FFFFFFFF
                                                    690
                                                    691 * Word
                                                    692          VRR_A VPOPCT,2
000013B8                                            693+         DS    0FD
000013B8                      000013B8              694+         USING *,R5               base for test data and test routine
000013B8  000013F8                                  695+T7       DC    A(X7)              address of test routine
000013BC  0007                                      696+         DC    H'7'               test number
000013BE  00                                        697+         DC    X'00'
000013BF  02                                        698+         DC    HL1'2'             M3
000013C0  E5D7D6D7 C3E34040                         699+         DC    CL8'VPOPCT'        instruction name
000013C8  00001424                                  700+         DC    A(RE7+16)          address of v2 source
000013CC  00000010                                  701+         DC    A(16)              result length
000013D0  00001414                                  702+REA7     DC    A(RE7)             result address
000013D8  00000000 00000000                         703+         DS    FD                 gap
000013E0  00000000 00000000                         704+V1O7     DS    XL16               V1 output
000013E8  00000000 00000000
000013F0  00000000 00000000                         705+         DS    FD                 gap
                                                    706+*
000013F8                                            707+X7       DS    0F
000013F8  E310 5010 0014                 00000010   708+         LGF   R1,V2ADDR          load v2 source
000013FE  E761 0000 0806                 00000000   709+         VL    v22,0(R1)          use v22 to test decoder
00001404  E766 0000 2C50                            710+         VPOPCT V22,V22,2         test instruction (dest is a source)
0000140A  E760 5028 080E                 000013E0   711+         VST   V22,V1O7           save v1 output
00001410  07FB                                      712+         BR    R11                return
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001414                                           713+RE7      DC    0F                  xl16 expected result
00001414                                           714+         DROP  R5
00001414  00000020 00000020                        715          DC    XL16'00000020000000200000002000000020'   expected result
0000141C  00000020 00000020
00001424  FFFFFFFF FFFFFFFF                        716          DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'   v2
0000142C  FFFFFFFF FFFFFFFF
                                                   717
                                                   718 * Doubleword
                                                   719          VRR_A VPOPCT,3
00001438                                           720+         DS    0FD
00001438                    00001438               721+         USING *,R5                base for test data and test routine
00001438  00001478                                 722+T8       DC    A(X8)               address of test routine
0000143C  0008                                     723+         DC    H'8'                test number
0000143E  00                                       724+         DC    X'00'
0000143F  03                                       725+         DC    HL1'3'              M3
00001440  E5D7D6D7 C3E34040                        726+         DC    CL8'VPOPCT'         instruction name
00001448  000014A4                                 727+         DC    A(RE8+16)           address of v2 source
0000144C  00000010                                 728+         DC    A(16)               result length
00001450  00001494                                 729+REA8     DC    A(RE8)              result address
00001458  00000000 00000000                        730+         DS    FD                  gap
00001460  00000000 00000000                        731+V1O8     DS    XL16                V1 output
00001468  00000000 00000000
00001470  00000000 00000000                        732+         DS    FD                  gap
                                                   733+*
00001478                                           734+X8       DS    0F
00001478  E310 5010 0014                00000010   735+         LGF   R1,V2ADDR           load v2 source
0000147E  E761 0000 0806                00000000   736+         VL    v22,0(R1)           use v22 to test decoder
00001484  E766 0000 3C50                           737+         VPOPCT V22,V22,3          test instruction (dest is a source)
0000148A  E760 5028 080E                00001460   738+         VST   V22,V1O8            save v1 output
00001490  07FB                                     739+         BR    R11                 return
00001494                                           740+RE8      DC    0F                  xl16 expected result
00001494                                           741+         DROP  R5
00001494  00000000 00000040                        742          DC    XL16'00000000000000400000000000000040'   expected result
0000149C  00000000 00000040
000014A4  FFFFFFFF FFFFFFFF                        743          DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'   v2
000014AC  FFFFFFFF FFFFFFFF
                                                   744
                                                   745 *-------------------------------------------------------------------
                                                   746 * case 1 - simple
                                                   747 *-------------------------------------------------------------------
                                                   748 * Byte
                                                   749          VRR_A VPOPCT,0
000014B8                                           750+         DS    0FD
000014B8                    000014B8               751+         USING *,R5                base for test data and test routine
000014B8  000014F8                                 752+T9       DC    A(X9)               address of test routine
000014BC  0009                                     753+         DC    H'9'                test number
000014BE  00                                       754+         DC    X'00'
000014BF  00                                       755+         DC    HL1'0'              M3
000014C0  E5D7D6D7 C3E34040                        756+         DC    CL8'VPOPCT'         instruction name
000014C8  00001524                                 757+         DC    A(RE9+16)           address of v2 source
000014CC  00000010                                 758+         DC    A(16)               result length
000014D0  00001514                                 759+REA9     DC    A(RE9)              result address
000014D8  00000000 00000000                        760+         DS    FD                  gap
000014E0  00000000 00000000                        761+V1O9     DS    XL16                V1 output
000014E8  00000000 00000000
000014F0  00000000 00000000                        762+         DS    FD                  gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    763+*
000014F8                                            764+X9       DS    0F
000014F8  E310 5010 0014                 00000010   765+         LGF   R1,V2ADDR          load v2 source
000014FE  E761 0000 0806                 00000000   766+         VL    v22,0(R1)         use v22 to test decoder
00001504  E766 0000 0C50                            767+         VPOPCT V22,V22,0        test instruction (dest is a source)
0000150A  E760 5028 080E                 000014E0   768+         VST   V22,V1O9          save v1 output
00001510  07FB                                      769+         BR    R11               return
00001514                                            770+RE9      DC    0F                xl16 expected result
00001514                                            771+         DROP  R5
00001514  00010102 01020203                         772          DC    XL16'00010102010202030102020302030304'   expected result
0000151C  01020203 02030304
00001524  00010203 04050607                         773          DC    XL16'000102030405060708090A0B0C0D0E0F'   v2
0000152C  08090A0B 0C0D0E0F
                                                    774
                                                    775 * Halfword
                                                    776          VRR_A VPOPCT,1
00001538                                            777+         DS    0FD
00001538                         00001538           778+         USING *,R5              base for test data and test routine
00001538  00001578                                  779+T10      DC    A(X10)            address of test routine
0000153C  000A                                      780+         DC    H'10'             test number
0000153E  00                                        781+         DC    X'00'
0000153F  01                                        782+         DC    HL1'1'            M3
00001540  E5D7D6D7 C3E34040                         783+         DC    CL8'VPOPCT'       instruction name
00001548  000015A4                                  784+         DC    A(RE10+16)        address of v2 source
0000154C  00000010                                  785+         DC    A(16)             result length
00001550  00001594                                  786+REA10    DC    A(RE10)           result address
00001558  00000000 00000000                         787+         DS    FD                gap
00001560  00000000 00000000                         788+V1O10    DS    XL16              V1 output
00001568  00000000 00000000
00001570  00000000 00000000                         789+         DS    FD                gap
                                                    790+*
00001578                                            791+X10      DS    0F
00001578  E310 5010 0014                 00000010   792+         LGF   R1,V2ADDR         load v2 source
0000157E  E761 0000 0806                 00000000   793+         VL    v22,0(R1)         use v22 to test decoder
00001584  E766 0000 1C50                            794+         VPOPCT V22,V22,1        test instruction (dest is a source)
0000158A  E760 5028 080E                 00001560   795+         VST   V22,V1O10         save v1 output
00001590  07FB                                      796+         BR    R11               return
00001594                                            797+RE10     DC    0F                xl16 expected result
00001594                                            798+         DROP  R5
00001594  00010003 00030005                         799          DC    XL16'00010003000300050003000500050007'   expected result
0000159C  00030005 00050007
000015A4  00010203 04050607                         800          DC    XL16'000102030405060708090A0B0C0D0E0F'   v2
000015AC  08090A0B 0C0D0E0F
                                                    801
                                                    802 * Word
                                                    803          VRR_A VPOPCT,2
000015B8                                            804+         DS    0FD
000015B8                         000015B8           805+         USING *,R5              base for test data and test routine
000015B8  000015F8                                  806+T11      DC    A(X11)            address of test routine
000015BC  000B                                      807+         DC    H'11'             test number
000015BE  00                                        808+         DC    X'00'
000015BF  02                                        809+         DC    HL1'2'            M3
000015C0  E5D7D6D7 C3E34040                         810+         DC    CL8'VPOPCT'       instruction name
000015C8  00001624                                  811+         DC    A(RE11+16)        address of v2 source
000015CC  00000010                                  812+         DC    A(16)             result length
000015D0  00001614                                  813+REA11    DC    A(RE11)           result address
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

000015D8  00000000 00000000                          814+         DS    FD                  gap
000015E0  00000000 00000000                          815+V1O11    DS    XL16                V1 output
000015E8  00000000 00000000
000015F0  00000000 00000000                          816+         DS    FD                  gap
                                                     817+*
000015F8                                             818+X11      DS    0F
000015F8  E310 5010 0014                 00000010    819+         LGF   R1,V2ADDR           load v2 source
000015FE  E761 0000 0806                 00000000    820+         VL    v22,0(R1)           use v22 to test decoder
00001604  E766 0000 2C50                             821+         VPOPCT V22,V22,2          test instruction (dest is a source)
0000160A  E760 5028 080E                 000015E0    822+         VST   V22,V1O11           save v1 output
00001610  07FB                                       823+         BR    R11                 return
00001614                                             824+RE11     DC    0F                  xl16 expected result
00001614                                             825+         DROP  R5
00001614  00000004 00000008                          826          DC    XL16'00000004000000080000000800000000C'   expected result
0000161C  00000008 0000000C
00001624  00010203 04050607                          827          DC    XL16'000102030405060708090A0B0C0D0E0F'   v2
0000162C  08090A0B 0C0D0E0F
                                                     828
                                                     829 * Doubleword
                                                     830          VRR_A VPOPCT,3
00001638                                             831+         DS    0FD
00001638                          00001638           832+         USING *,R5                base for test data and test routine
00001638  00001678                                   833+T12      DC    A(X12)              address of test routine
0000163C  000C                                       834+         DC    H'12'               test number
0000163E  00                                         835+         DC    X'00'
0000163F  03                                         836+         DC    HL1'3'              M3
00001640  E5D7D6D7 C3E34040                          837+         DC    CL8'VPOPCT'         instruction name
00001648  000016A4                                   838+         DC    A(RE12+16)          address of v2 source
0000164C  00000010                                   839+         DC    A(16)               result length
00001650  00001694                                   840+REA12    DC    A(RE12)             result address
00001658  00000000 00000000                          841+         DS    FD                  gap
00001660  00000000 00000000                          842+V1O12    DS    XL16                V1 output
00001668  00000000 00000000
00001670  00000000 00000000                          843+         DS    FD                  gap
                                                     844+*
00001678                                             845+X12      DS    0F
00001678  E310 5010 0014                 00000010    846+         LGF   R1,V2ADDR           load v2 source
0000167E  E761 0000 0806                 00000000    847+         VL    v22,0(R1)           use v22 to test decoder
00001684  E766 0000 3C50                             848+         VPOPCT V22,V22,3          test instruction (dest is a source)
0000168A  E760 5028 080E                 00001660    849+         VST   V22,V1O12           save v1 output
00001690  07FB                                       850+         BR    R11                 return
00001694                                             851+RE12     DC    0F                  xl16 expected result
00001694                                             852+         DROP  R5
00001694  00000000 0000000C                          853          DC    XL16'00000000000000C0000000000000014'   expected result
0000169C  00000000 00000014
000016A4  00010203 04050607                          854          DC    XL16'000102030405060708090A0B0C0D0E0F'   v2
000016AC  08090A0B 0C0D0E0F
                                                     855
                                                     856 *-------------------------------------------------------------------
                                                     857 * case 2 - hw verified
                                                     858 *-------------------------------------------------------------------
                                                     859 * Byte
                                                     860          VRR_A VPOPCT,0
000016B8                                             861+         DS    0FD
000016B8                          000016B8           862+         USING *,R5                base for test data and test routine
000016B8  000016F8                                   863+T13      DC    A(X13)              address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000016BC  000D                                     864+          DC    H'13'               test number
000016BE  00                                       865+          DC    X'00'
000016BF  00                                       866+          DC    HL1'0'              M3
000016C0  E5D7D6D7 C3E34040                        867+          DC    CL8'VPOPCT'         instruction name
000016C8  00001724                                 868+          DC    A(RE13+16)          address of v2 source
000016CC  00000010                                 869+          DC    A(16)               result length
000016D0  00001714                                 870+REA13     DC    A(RE13)             result address
000016D8  00000000 00000000                        871+          DS    FD                  gap
000016E0  00000000 00000000                        872+V1O13     DS    XL16                V1 output
000016E8  00000000 00000000
000016F0  00000000 00000000                        873+          DS    FD                  gap
                                                   874+*
000016F8                                           875+X13       DS    0F
000016F8  E310 5010 0014                 00000010  876+          LGF   R1,V2ADDR           load v2 source
000016FE  E761 0000 0806                 00000000  877+          VL    v22,0(R1)           use v22 to test decoder
00001704  E766 0000 0C50                           878+          VPOPCT V22,V22,0          test instruction (dest is a source)
0000170A  E760 5028 080E                 000016E0  879+          VST   V22,V1O13           save v1 output
00001710  07FB                                     880+          BR    R11                 return
00001714                                           881+RE13      DC    0F                  xl16 expected result
00001714                                           882+          DROP  R5
00001714  00080202 00080303                        883           DC    XL16'00080202000803030008050500080505'   expected result
0000171C  00080505 00080505
00001724  00FF8811 00FF43C2                        884           DC    XL16'00FF881100FF43C200FFF42F00FF37EC'   v2
0000172C  00FFF42F 00FF37EC
                                                   885
                                                   886 * Halfword
00001738                                           887           VRR_A VPOPCT,1
00001738                                           888+          DS    0FD
00001738                         00001738          889+          USING *,R5                base for test data and test routine
00001738  00001778                                 890+T14       DC    A(X14)              address of test routine
0000173C  000E                                     891+          DC    H'14'               test number
0000173E  00                                       892+          DC    X'00'
0000173F  01                                       893+          DC    HL1'1'              M3
00001740  E5D7D6D7 C3E34040                        894+          DC    CL8'VPOPCT'         instruction name
00001748  000017A4                                 895+          DC    A(RE14+16)          address of v2 source
0000174C  00000010                                 896+          DC    A(16)               result length
00001750  00001794                                 897+REA14     DC    A(RE14)             result address
00001758  00000000 00000000                        898+          DS    FD                  gap
00001760  00000000 00000000                        899+V1O14     DS    XL16                V1 output
00001768  00000000 00000000
00001770  00000000 00000000                        900+          DS    FD                  gap
                                                   901+*
00001778                                           902+X14       DS    0F
00001778  E310 5010 0014                 00000010  903+          LGF   R1,V2ADDR           load v2 source
0000177E  E761 0000 0806                 00000000  904+          VL    v22,0(R1)           use v22 to test decoder
00001784  E766 0000 1C50                           905+          VPOPCT V22,V22,1          test instruction (dest is a source)
0000178A  E760 5028 080E                 00001760  906+          VST   V22,V1O14           save v1 output
00001790  07FB                                     907+          BR    R11                 return
00001794                                           908+RE14      DC    0F                  xl16 expected result
00001794                                           909+          DROP  R5
00001794  00000010 00020002                        910           DC    XL16'00000010000200020000001000040006'   expected result
0000179C  00000010 00040006
000017A4  0000FFFF 08800110                        911           DC    XL16'0000FFFF088001100000FFFF0660468A'   v2
000017AC  0000FFFF 0660468A
                                                   912
                                                   913 * Word
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     914          VRR_A VPOPCT,2
000017B8                                             915+         DS    0FD
000017B8                       000017B8              916+         USING *,R5              base for test data and test routine
000017B8  000017F8                                   917+T15      DC    A(X15)            address of test routine
000017BC  000F                                       918+         DC    H'15'             test number
000017BE  00                                         919+         DC    X'00'
000017BF  02                                         920+         DC    HL1'2'            M3
000017C0  E5D7D6D7 C3E34040                          921+         DC    CL8'VPOPCT'       instruction name
000017C8  00001824                                   922+         DC    A(RE15+16)        address of v2 source
000017CC  00000010                                   923+         DC    A(16)             result length
000017D0  00001814                                   924+REA15    DC    A(RE15)           result address
000017D8  00000000 00000000                          925+         DS    FD                gap
000017E0  00000000 00000000                          926+V1O15    DS    XL16              V1 output
000017E8  00000000 00000000
000017F0  00000000 00000000                          927+         DS    FD                gap
                                                     928+*
000017F8                                             929+X15      DS    0F
000017F8  E310 5010 0014                 00000010    930+         LGF   R1,V2ADDR         load v2 source
000017FE  E761 0000 0806                 00000000    931+         VL    v22,0(R1)         use v22 to test decoder
00001804  E766 0000 2C50                             932+         VPOPCT V22,V22,2        test instruction (dest is a source)
0000180A  E760 5028 080E                 000017E0    933+         VST   V22,V1O15         save v1 output
00001810  07FB                                       934+         BR    R11               return
00001814                                             935+RE15     DC    0F                xl16 expected result
00001814                                             936+         DROP  R5
00001814  00000000 00000020                          937          DC    XL16'00000000000000200000000200000002'   expected result
0000181C  00000002 00000002
00001824  00000000 FFFFFFFF                          938          DC    XL16'00000000FFFFFFFF0080800000011000'   v2
0000182C  00808000 00011000
                                                     939
                                                     940 * Doubleword
                                                     941          VRR_A VPOPCT,3
00001838                                             942+         DS    0FD
00001838                       00001838              943+         USING *,R5              base for test data and test routine
00001838  00001878                                   944+T16      DC    A(X16)            address of test routine
0000183C  0010                                       945+         DC    H'16'             test number
0000183E  00                                         946+         DC    X'00'
0000183F  03                                         947+         DC    HL1'3'            M3
00001840  E5D7D6D7 C3E34040                          948+         DC    CL8'VPOPCT'       instruction name
00001848  000018A4                                   949+         DC    A(RE16+16)        address of v2 source
0000184C  00000010                                   950+         DC    A(16)             result length
00001850  00001894                                   951+REA16    DC    A(RE16)           result address
00001858  00000000 00000000                          952+         DS    FD                gap
00001860  00000000 00000000                          953+V1O16    DS    XL16              V1 output
00001868  00000000 00000000
00001870  00000000 00000000                          954+         DS    FD                gap
                                                     955+*
00001878                                             956+X16      DS    0F
00001878  E310 5010 0014                 00000010    957+         LGF   R1,V2ADDR         load v2 source
0000187E  E761 0000 0806                 00000000    958+         VL    v22,0(R1)         use v22 to test decoder
00001884  E766 0000 3C50                             959+         VPOPCT V22,V22,3        test instruction (dest is a source)
0000188A  E760 5028 080E                 00001860    960+         VST   V22,V1O16         save v1 output
00001890  07FB                                       961+         BR    R11               return
00001894                                             962+RE16     DC    0F                xl16 expected result
00001894                                             963+         DROP  R5
00001894  00000000 00000000                          964          DC    XL16'00000000000000000000000000000040'   expected result
0000189C  00000000 00000040
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000018A4  00000000 00000000                        965          DC    XL16'0000000000000000FFFFFFFFFFFFFFFF'   v2
000018AC  FFFFFFFF FFFFFFFF
                                                   966
                                                   967 * Doubleword
                                                   968          VRR_A VPOPCT,3
000018B8                                           969+         DS    0FD
000018B8                     000018B8              970+         USING *,R5               base for test data and test routine
000018B8  000018F8                                 971+T17      DC    A(X17)             address of test routine
000018BC  0011                                     972+         DC    H'17'              test number
000018BE  00                                       973+         DC    X'00'
000018BF  03                                       974+         DC    HL1'3'             M3
000018C0  E5D7D6D7 C3E34040                        975+         DC    CL8'VPOPCT'        instruction name
000018C8  00001924                                 976+         DC    A(RE17+16)         address of v2 source
000018CC  00000010                                 977+         DC    A(16)              result length
000018D0  00001914                                 978+REA17    DC    A(RE17)            result address
000018D8  00000000 00000000                        979+         DS    FD                 gap
000018E0  00000000 00000000                        980+V1O17    DS    XL16               V1 output
000018E8  00000000 00000000
000018F0  00000000 00000000                        981+         DS    FD                 gap
                                                   982+*
000018F8                                           983+X17      DS    0F
000018F8  E310 5010 0014                 00000010  984+         LGF   R1,V2ADDR          load v2 source
000018FE  E761 0000 0806                 00000000  985+         VL    v22,0(R1)          use v22 to test decoder
00001904  E766 0000 3C50                           986+         VPOPCT V22,V22,3         test instruction (dest is a source)
0000190A  E760 5028 080E                 000018E0  987+         VST   V22,V1O17          save v1 output
00001910  07FB                                     988+         BR    R11                return
00001914                                           989+RE17     DC    0F                 xl16 expected result
00001914                                           990+         DROP  R5
00001914  00000000 00000001                        991          DC    XL16'00000000000000010000000000000002'   expected result
0000191C  00000000 00000002
00001924  00000000 00800000                        992          DC    XL16'00000000008000000000000001100000'   v2
0000192C  00000000 01100000
                                                   993
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    995 *================================================================================
                                                    996 *--------------------------------------------------------------------------------
                                                    997 * VCTZ   - Vector Count Trailing Zeros
                                                    998 *--------------------------------------------------------------------------------
                                                    999
                                                   1000 *--------------------------------------------------------------------------------
                                                   1001 * case 0 - simple, simple debug
                                                   1002 *--------------------------------------------------------------------------------
                                                   1003 * Byte
                                                   1004          VRR_A VCTZ,0
00001938                                           1005+         DS    0FD
00001938                       00001938            1006+         USING *,R5                base for test data and test routine
00001938  00001978                                 1007+T18      DC    A(X18)              address of test routine
0000193C  0012                                     1008+         DC    H'18'               test number
0000193E  00                                       1009+         DC    X'00'
0000193F  00                                       1010+         DC    HL1'0'              M3
00001940  E5C3E3E9 40404040                        1011+         DC    CL8'VCTZ'           instruction name
00001948  000019A4                                 1012+         DC    A(RE18+16)          address of v2 source
0000194C  00000010                                 1013+         DC    A(16)               result length
00001950  00001994                                 1014+REA18    DC    A(RE18)             result address
00001958  00000000 00000000                        1015+         DS    FD                  gap
00001960  00000000 00000000                        1016+V1O18    DS    XL16                V1 output
00001968  00000000 00000000
00001970  00000000 00000000                        1017+         DS    FD                  gap
                                                   1018+*
00001978                                           1019+X18      DS    0F
00001978  E310 5010 0014                00000010   1020+         LGF   R1,V2ADDR           load v2 source
0000197E  E761 0000 0806                00000000   1021+         VL    v22,0(R1)           use v22 to test decoder
00001984  E766 0000 0C52                           1022+         VCTZ  V22,V22,0           test instruction (dest is a source)
0000198A  E760 5028 080E                00001960   1023+         VST   V22,V1O18           save v1 output
00001990  07FB                                     1024+         BR    R11                 return
00001994                                           1025+RE18     DC    0F                  xl16 expected result
00001994                                           1026+         DROP  R5
00001994  08080808 08080808                        1027          DC    XL16'08080808080808080808080808080808'   expected result
0000199C  08080808 08080808
000019A4  00000000 00000000                        1028          DC    XL16'00000000000000000000000000000000'   v2
000019AC  00000000 00000000
                                                   1029
                                                   1030 * Halfword
                                                   1031          VRR_A VCTZ,1
000019B8                                           1032+         DS    0FD
000019B8                       000019B8            1033+         USING *,R5                base for test data and test routine
000019B8  000019F8                                 1034+T19      DC    A(X19)              address of test routine
000019BC  0013                                     1035+         DC    H'19'               test number
000019BE  00                                       1036+         DC    X'00'
000019BF  01                                       1037+         DC    HL1'1'              M3
000019C0  E5C3E3E9 40404040                        1038+         DC    CL8'VCTZ'           instruction name
000019C8  00001A24                                 1039+         DC    A(RE19+16)          address of v2 source
000019CC  00000010                                 1040+         DC    A(16)               result length
000019D0  00001A14                                 1041+REA19    DC    A(RE19)             result address
000019D8  00000000 00000000                        1042+         DS    FD                  gap
000019E0  00000000 00000000                        1043+V1O19    DS    XL16                V1 output
000019E8  00000000 00000000
000019F0  00000000 00000000                        1044+         DS    FD                  gap
                                                   1045+*
000019F8                                           1046+X19      DS    0F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000019F8  E310 5010 0014                 00000010  1047+          LGF   R1,V2ADDR           load v2 source
000019FE  E761 0000 0806                 00000000  1048+          VL    v22,0(R1)           use v22 to test decoder
00001A04  E766 0000 1C52                           1049+          VCTZ  V22,V22,1           test instruction (dest is a source)
00001A0A  E760 5028 080E                 000019E0  1050+          VST   V22,V1O19           save v1 output
00001A10  07FB                                     1051+          BR    R11                 return
00001A14                                           1052+RE19      DC    0F                  xl16 expected result
00001A14                                           1053+          DROP  R5
00001A14  00100010 00100010                        1054           DC    XL16'00100010001000100010001000100010'   expected result
00001A1C  00100010 00100010
00001A24  00000000 00000000                        1055           DC    XL16'00000000000000000000000000000000'   v2
00001A2C  00000000 00000000
                                                   1056
                                                   1057 * Word
                                                   1058           VRR_A VCTZ,2
00001A38                                           1059+          DS    0FD
00001A38                           00001A38        1060+          USING *,R5                base for test data and test routine
00001A38  00001A78                                 1061+T20       DC    A(X20)              address of test routine
00001A3C  0014                                     1062+          DC    H'20'               test number
00001A3E  00                                       1063+          DC    X'00'
00001A3F  02                                       1064+          DC    HL1'2'              M3
00001A40  E5C3E3E9 40404040                        1065+          DC    CL8'VCTZ'           instruction name
00001A48  00001AA4                                 1066+          DC    A(RE20+16)          address of v2 source
00001A4C  00000010                                 1067+          DC    A(16)               result length
00001A50  00001A94                                 1068+REA20     DC    A(RE20)             result address
00001A58  00000000 00000000                        1069+          DS    FD                  gap
00001A60  00000000 00000000                        1070+V1O20     DS    XL16                V1 output
00001A68  00000000 00000000
00001A70  00000000 00000000                        1071+          DS    FD                  gap
                                                   1072+*
00001A78                                           1073+X20       DS    0F
00001A78  E310 5010 0014                 00000010  1074+          LGF   R1,V2ADDR           load v2 source
00001A7E  E761 0000 0806                 00000000  1075+          VL    v22,0(R1)           use v22 to test decoder
00001A84  E766 0000 2C52                           1076+          VCTZ  V22,V22,2           test instruction (dest is a source)
00001A8A  E760 5028 080E                 00001A60  1077+          VST   V22,V1O20           save v1 output
00001A90  07FB                                     1078+          BR    R11                 return
00001A94                                           1079+RE20      DC    0F                  xl16 expected result
00001A94                                           1080+          DROP  R5
00001A94  00000020 00000020                        1081           DC    XL16'00000020000000200000002000000020'   expected result
00001A9C  00000020 00000020
00001AA4  00000000 00000000                        1082           DC    XL16'00000000000000000000000000000000'   v2
00001AAC  00000000 00000000
                                                   1083
                                                   1084 * Doubleword
                                                   1085           VRR_A VCTZ,3
00001AB8                                           1086+          DS    0FD
00001AB8                           00001AB8        1087+          USING *,R5                base for test data and test routine
00001AB8  00001AF8                                 1088+T21       DC    A(X21)              address of test routine
00001ABC  0015                                     1089+          DC    H'21'               test number
00001ABE  00                                       1090+          DC    X'00'
00001ABF  03                                       1091+          DC    HL1'3'              M3
00001AC0  E5C3E3E9 40404040                        1092+          DC    CL8'VCTZ'           instruction name
00001AC8  00001B24                                 1093+          DC    A(RE21+16)          address of v2 source
00001ACC  00000010                                 1094+          DC    A(16)               result length
00001AD0  00001B14                                 1095+REA21     DC    A(RE21)             result address
00001AD8  00000000 00000000                        1096+          DS    FD                  gap
00001AE0  00000000 00000000                        1097+V1O21     DS    XL16                V1 output
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
00001AE8  00000000 00000000
00001AF0  00000000 00000000                       1098+         DS    FD                gap
                                                  1099+*
00001AF8                                          1100+X21      DS    0F
00001AF8  E310 5010 0014                 00000010 1101+         LGF   R1,V2ADDR         load v2 source
00001AFE  E761 0000 0806                 00000000 1102+         VL    v22,0(R1)         use v22 to test decoder
00001B04  E766 0000 3C52                          1103+         VCTZ  V22,V22,3         test instruction (dest is a source)
00001B0A  E760 5028 080E                 00001AE0 1104+         VST   V22,V1O21         save v1 output
00001B10  07FB                                    1105+         BR    R11               return
00001B14                                          1106+RE21     DC    0F                xl16 expected result
00001B14                                          1107+         DROP  R5
00001B14  00000000 00000040                       1108          DC    XL16'00000000000000400000000000000040'   expected result
00001B1C  00000000 00000040
00001B24  00000000 00000000                       1109          DC    XL16'00000000000000000000000000000000'   v2
00001B2C  00000000 00000000
                                                  1110
                                                  1111 *-------------------------------------------------------------------
                                                  1112 * Byte
                                                  1113          VRR_A VCTZ,0
00001B38                                          1114+         DS    0FD
00001B38                          00001B38        1115+         USING *,R5              base for test data and test routine
00001B38  00001B78                                1116+T22      DC    A(X22)            address of test routine
00001B3C  0016                                    1117+         DC    H'22'             test number
00001B3E  00                                      1118+         DC    X'00'
00001B3F  00                                      1119+         DC    HL1'0'            M3
00001B40  E5C3E3E9 40404040                       1120+         DC    CL8'VCTZ'         instruction name
00001B48  00001BA4                                1121+         DC    A(RE22+16)        address of v2 source
00001B4C  00000010                                1122+         DC    A(16)             result length
00001B50  00001B94                                1123+REA22    DC    A(RE22)           result address
00001B58  00000000 00000000                       1124+         DS    FD                gap
00001B60  00000000 00000000                       1125+V1O22    DS    XL16              V1 output
00001B68  00000000 00000000
00001B70  00000000 00000000                       1126+         DS    FD                gap
                                                  1127+*
00001B78                                          1128+X22      DS    0F
00001B78  E310 5010 0014                 00000010 1129+         LGF   R1,V2ADDR         load v2 source
00001B7E  E761 0000 0806                 00000000 1130+         VL    v22,0(R1)         use v22 to test decoder
00001B84  E766 0000 0C52                          1131+         VCTZ  V22,V22,0         test instruction (dest is a source)
00001B8A  E760 5028 080E                 00001B60 1132+         VST   V22,V1O22         save v1 output
00001B90  07FB                                    1133+         BR    R11               return
00001B94                                          1134+RE22     DC    0F                xl16 expected result
00001B94                                          1135+         DROP  R5
00001B94  00000000 00000000                       1136          DC    XL16'00000000000000000000000000000000'   expected result
00001B9C  00000000 00000000
00001BA4  FFFFFFFF FFFFFFFF                       1137          DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'   v2
00001BAC  FFFFFFFF FFFFFFFF
                                                  1138
                                                  1139 * Halfword
                                                  1140          VRR_A VCTZ,1
00001BB8                                          1141+         DS    0FD
00001BB8                          00001BB8        1142+         USING *,R5              base for test data and test routine
00001BB8  00001BF8                                1143+T23      DC    A(X23)            address of test routine
00001BBC  0017                                    1144+         DC    H'23'             test number
00001BBE  00                                      1145+         DC    X'00'
00001BBF  01                                      1146+         DC    HL1'1'            M3
00001BC0  E5C3E3E9 40404040                       1147+         DC    CL8'VCTZ'         instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001BC8  00001C24                             1148+          DC    A(RE23+16)          address of v2 source
00001BCC  00000010                             1149+          DC    A(16)               result length
00001BD0  00001C14                             1150+REA23     DC    A(RE23)             result address
00001BD8  00000000 00000000                    1151+          DS    FD                  gap
00001BE0  00000000 00000000                    1152+V1O23     DS    XL16                V1 output
00001BE8  00000000 00000000
00001BF0  00000000 00000000                    1153+          DS    FD                  gap
                                               1154+*
00001BF8                                       1155+X23       DS    0F
00001BF8  E310 5010 0014             00000010  1156+          LGF   R1,V2ADDR           load v2 source
00001BFE  E761 0000 0806             00000000  1157+          VL    v22,0(R1)           use v22 to test decoder
00001C04  E766 0000 1C52                       1158+          VCTZ  V22,V22,1           test instruction (dest is a source)
00001C0A  E760 5028 080E             00001BE0  1159+          VST   V22,V1O23           save v1 output
00001C10  07FB                                 1160+          BR    R11                 return
00001C14                                       1161+RE23      DC    0F                  xl16 expected result
00001C14                                       1162+          DROP  R5
00001C14  00000000 00000000                    1163           DC    XL16'00000000000000000000000000000000'   expected result
00001C1C  00000000 00000000
00001C24  FFFFFFFF FFFFFFFF                    1164           DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'   v2
00001C2C  FFFFFFFF FFFFFFFF
                                               1165
                                               1166 * Word
                                               1167           VRR_A VCTZ,2
00001C38                                       1168+          DS    0FD
00001C38                       00001C38        1169+          USING *,R5                base for test data and test routine
00001C38  00001C78                             1170+T24       DC    A(X24)              address of test routine
00001C3C  0018                                 1171+          DC    H'24'               test number
00001C3E  00                                   1172+          DC    X'00'
00001C3F  02                                   1173+          DC    HL1'2'              M3
00001C40  E5C3E3E9 40404040                    1174+          DC    CL8'VCTZ'           instruction name
00001C48  00001CA4                             1175+          DC    A(RE24+16)          address of v2 source
00001C4C  00000010                             1176+          DC    A(16)               result length
00001C50  00001C94                             1177+REA24     DC    A(RE24)             result address
00001C58  00000000 00000000                    1178+          DS    FD                  gap
00001C60  00000000 00000000                    1179+V1O24     DS    XL16                V1 output
00001C68  00000000 00000000
00001C70  00000000 00000000                    1180+          DS    FD                  gap
                                               1181+*
00001C78                                       1182+X24       DS    0F
00001C78  E310 5010 0014             00000010  1183+          LGF   R1,V2ADDR           load v2 source
00001C7E  E761 0000 0806             00000000  1184+          VL    v22,0(R1)           use v22 to test decoder
00001C84  E766 0000 2C52                       1185+          VCTZ  V22,V22,2           test instruction (dest is a source)
00001C8A  E760 5028 080E             00001C60  1186+          VST   V22,V1O24           save v1 output
00001C90  07FB                                 1187+          BR    R11                 return
00001C94                                       1188+RE24      DC    0F                  xl16 expected result
00001C94                                       1189+          DROP  R5
00001C94  00000000 00000000                    1190           DC    XL16'00000000000000000000000000000000'   expected result
00001C9C  00000000 00000000
00001CA4  FFFFFFFF FFFFFFFF                    1191           DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'   v2
00001CAC  FFFFFFFF FFFFFFFF
                                               1192
                                               1193 * Doubleword
                                               1194           VRR_A VCTZ,3
00001CB8                                       1195+          DS    0FD
00001CB8                       00001CB8        1196+          USING *,R5                base for test data and test routine
00001CB8  00001CF8                             1197+T25       DC    A(X25)              address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001CBC  0019                                     1198+          DC    H'25'               test number
00001CBE  00                                       1199+          DC    X'00'
00001CBF  03                                       1200+          DC    HL1'3'              M3
00001CC0  E5C3E3E9 40404040                        1201+          DC    CL8'VCTZ'           instruction name
00001CC8  00001D24                                 1202+          DC    A(RE25+16)          address of v2 source
00001CCC  00000010                                 1203+          DC    A(16)               result length
00001CD0  00001D14                                 1204+REA25     DC    A(RE25)             result address
00001CD8  00000000 00000000                        1205+          DS    FD                  gap
00001CE0  00000000 00000000                        1206+V1O25     DS    XL16                V1 output
00001CE8  00000000 00000000
00001CF0  00000000 00000000                        1207+          DS    FD                  gap
                                                   1208+*
00001CF8                                           1209+X25       DS    0F
00001CF8  E310 5010 0014                 00000010  1210+          LGF   R1,V2ADDR           load v2 source
00001CFE  E761 0000 0806                 00000000  1211+          VL    v22,0(R1)           use v22 to test decoder
00001D04  E766 0000 3C52                           1212+          VCTZ  V22,V22,3           test instruction (dest is a source)
00001D0A  E760 5028 080E                 00001CE0  1213+          VST   V22,V1O25           save v1 output
00001D10  07FB                                     1214+          BR    R11                 return
00001D14                                           1215+RE25      DC    0F                  xl16 expected result
00001D14                                           1216+          DROP  R5
00001D14  00000000 00000000                        1217           DC    XL16'00000000000000000000000000000000'   expected result
00001D1C  00000000 00000000
00001D24  FFFFFFFF FFFFFFFF                        1218           DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'   v2
00001D2C  FFFFFFFF FFFFFFFF
                                                   1219
                                                   1220 *-------------------------------------------------------------------
                                                   1221 * case 1 - simple
                                                   1222 *-------------------------------------------------------------------
                                                   1223 * Byte
                                                   1224           VRR_A VCTZ,0
00001D38                                           1225+          DS    0FD
00001D38                         00001D38          1226+          USING *,R5                base for test data and test routine
00001D38  00001D78                                 1227+T26       DC    A(X26)              address of test routine
00001D3C  001A                                     1228+          DC    H'26'               test number
00001D3E  00                                       1229+          DC    X'00'
00001D3F  00                                       1230+          DC    HL1'0'              M3
00001D40  E5C3E3E9 40404040                        1231+          DC    CL8'VCTZ'           instruction name
00001D48  00001DA4                                 1232+          DC    A(RE26+16)          address of v2 source
00001D4C  00000010                                 1233+          DC    A(16)               result length
00001D50  00001D94                                 1234+REA26     DC    A(RE26)             result address
00001D58  00000000 00000000                        1235+          DS    FD                  gap
00001D60  00000000 00000000                        1236+V1O26     DS    XL16                V1 output
00001D68  00000000 00000000
00001D70  00000000 00000000                        1237+          DS    FD                  gap
                                                   1238+*
00001D78                                           1239+X26       DS    0F
00001D78  E310 5010 0014                 00000010  1240+          LGF   R1,V2ADDR           load v2 source
00001D7E  E761 0000 0806                 00000000  1241+          VL    v22,0(R1)           use v22 to test decoder
00001D84  E766 0000 0C52                           1242+          VCTZ  V22,V22,0           test instruction (dest is a source)
00001D8A  E760 5028 080E                 00001D60  1243+          VST   V22,V1O26           save v1 output
00001D90  07FB                                     1244+          BR    R11                 return
00001D94                                           1245+RE26      DC    0F                  xl16 expected result
00001D94                                           1246+          DROP  R5
00001D94  08000100 02000100                        1247           DC    XL16'08000100020001000300010002000100'   expected result
00001D9C  03000100 02000100
00001DA4  00010203 04050607                        1248           DC    XL16'000102030405060708090A0B0C0D0E0F'   v2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001DAC  08090A0B 0C0D0E0F                          1249
                                                     1250 * Halfword
                                                     1251          VRR_A VCTZ,1
00001DB8                                             1252+         DS    0FD
00001DB8                            00001DB8         1253+         USING *,R5              base for test data and test routine
00001DB8  00001DF8                                   1254+T27      DC    A(X27)            address of test routine
00001DBC  001B                                       1255+         DC    H'27'             test number
00001DBE  00                                         1256+         DC    X'00'
00001DBF  01                                         1257+         DC    HL1'1'            M3
00001DC0  E5C3E3E9 40404040                          1258+         DC    CL8'VCTZ'         instruction name
00001DC8  00001E24                                   1259+         DC    A(RE27+16)        address of v2 source
00001DCC  00000010                                   1260+         DC    A(16)             result length
00001DD0  00001E14                                   1261+REA27    DC    A(RE27)           result address
00001DD8  00000000 00000000                          1262+         DS    FD                gap
00001DE0  00000000 00000000                          1263+V1O27    DS    XL16              V1 output
00001DE8  00000000 00000000
00001DF0  00000000 00000000                          1264+         DS    FD                gap
                                                     1265+*
00001DF8                                             1266+X27      DS    0F
00001DF8  E310 5010 0014                 00000010    1267+         LGF   R1,V2ADDR         load v2 source
00001DFE  E761 0000 0806                 00000000    1268+         VL    v22,0(R1)         use v22 to test decoder
00001E04  E766 0000 1C52                             1269+         VCTZ  V22,V22,1         test instruction (dest is a source)
00001E0A  E760 5028 080E                 00001DE0    1270+         VST   V22,V1O27         save v1 output
00001E10  07FB                                       1271+         BR    R11               return
00001E14                                             1272+RE27     DC    0F                xl16 expected result
00001E14  00000001 00080008                          1273+         DROP  R5
00001E14  00080007 000C0004                          1274          DC    XL16'00000001000800080008007000C0004'   expected result
00001E24  FEDBFEDA F500F100                          1275          DC    XL16'FEDBFEDAF500F100F300F880F000FED0'   v2
00001E2C  F300F880 F000FED0
                                                     1276
                                                     1277 * Word
                                                     1278          VRR_A VCTZ,2
00001E38                                             1279+         DS    0FD
00001E38                            00001E38         1280+         USING *,R5              base for test data and test routine
00001E38  00001E78                                   1281+T28      DC    A(X28)            address of test routine
00001E3C  001C                                       1282+         DC    H'28'             test number
00001E3E  00                                         1283+         DC    X'00'
00001E3F  02                                         1284+         DC    HL1'2'            M3
00001E40  E5C3E3E9 40404040                          1285+         DC    CL8'VCTZ'         instruction name
00001E48  00001EA4                                   1286+         DC    A(RE28+16)        address of v2 source
00001E4C  00000010                                   1287+         DC    A(16)             result length
00001E50  00001E94                                   1288+REA28    DC    A(RE28)           result address
00001E58  00000000 00000000                          1289+         DS    FD                gap
00001E60  00000000 00000000                          1290+V1O28    DS    XL16              V1 output
00001E68  00000000 00000000
00001E70  00000000 00000000                          1291+         DS    FD                gap
                                                     1292+*
00001E78                                             1293+X28      DS    0F
00001E78  E310 5010 0014                 00000010    1294+         LGF   R1,V2ADDR         load v2 source
00001E7E  E761 0000 0806                 00000000    1295+         VL    v22,0(R1)         use v22 to test decoder
00001E84  E766 0000 2C52                             1296+         VCTZ  V22,V22,2         test instruction (dest is a source)
00001E8A  E760 5028 080E                 00001E60    1297+         VST   V22,V1O28         save v1 output
00001E90  07FB                                       1298+         BR    R11               return
00001E94                                             1299+RE28     DC    0F                xl16 expected result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001E94                                           1300+          DROP  R5
00001E94  00000001 00000008                        1301           DC    XL16'00000001000000080000000700000004'   expected result
00001E9C  00000007 00000004
00001EA4  FEDBFEDA F500F100                        1302           DC    XL16'FEDBFEDAF500F100F300F880F000FED0'   v2
00001EAC  F300F880 F000FED0
                                                   1303
                                                   1304 * Doubleword
                                                   1305           VRR_A VCTZ,3
00001EB8                                           1306+          DS    0FD
00001EB8                    00001EB8               1307+          USING *,R5               base for test data and test routine
00001EB8  00001EF8                                 1308+T29       DC    A(X29)             address of test routine
00001EBC  001D                                     1309+          DC    H'29'              test number
00001EBE  00                                       1310+          DC    X'00'
00001EBF  03                                       1311+          DC    HL1'3'             M3
00001EC0  E5C3E3E9 40404040                        1312+          DC    CL8'VCTZ'          instruction name
00001EC8  00001F24                                 1313+          DC    A(RE29+16)         address of v2 source
00001ECC  00000010                                 1314+          DC    A(16)              result length
00001ED0  00001F14                                 1315+REA29     DC    A(RE29)            result address
00001ED8  00000000 00000000                        1316+          DS    FD                 gap
00001EE0  00000000 00000000                        1317+V1O29     DS    XL16               V1 output
00001EE8  00000000 00000000
00001EF0  00000000 00000000                        1318+          DS    FD                 gap
                                                   1319+*
00001EF8                                           1320+X29       DS    0F
00001EF8  E310 5010 0014                00000010   1321+          LGF   R1,V2ADDR          load v2 source
00001EFE  E761 0000 0806                00000000   1322+          VL    v22,0(R1)          use v22 to test decoder
00001F04  E766 0000 3C52                           1323+          VCTZ  V22,V22,3          test instruction (dest is a source)
00001F0A  E760 5028 080E                00001EE0   1324+          VST   V22,V1O29          save v1 output
00001F10  07FB                                     1325+          BR    R11                return
00001F14                                           1326+RE29      DC    0F                 xl16 expected result
00001F14                                           1327+          DROP  R5
00001F14  00000000 00000008                        1328           DC    XL16'00000000000000080000000000000004'   expected result
00001F1C  00000000 00000004
00001F24  FEDBFEDA F500F100                        1329           DC    XL16'FEDBFEDAF500F100F300F880F000FED0'   v2
00001F2C  F300F880 F000FED0
                                                   1330
                                                   1331 *-------------------------------------------------------------------
                                                   1332 * case 2 - hw verified
                                                   1333 *-------------------------------------------------------------------
                                                   1334 * Byte
                                                   1335           VRR_A VCTZ,0
00001F38                                           1336+          DS    0FD
00001F38                    00001F38               1337+          USING *,R5               base for test data and test routine
00001F38  00001F78                                 1338+T30       DC    A(X30)             address of test routine
00001F3C  001E                                     1339+          DC    H'30'              test number
00001F3E  00                                       1340+          DC    X'00'
00001F3F  00                                       1341+          DC    HL1'0'             M3
00001F40  E5C3E3E9 40404040                        1342+          DC    CL8'VCTZ'          instruction name
00001F48  00001FA4                                 1343+          DC    A(RE30+16)         address of v2 source
00001F4C  00000010                                 1344+          DC    A(16)              result length
00001F50  00001F94                                 1345+REA30     DC    A(RE30)            result address
00001F58  00000000 00000000                        1346+          DS    FD                 gap
00001F60  00000000 00000000                        1347+V1O30     DS    XL16               V1 output
00001F68  00000000 00000000
00001F70  00000000 00000000                        1348+          DS    FD                 gap
                                                   1349+*
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001F78                                           1350+X30      DS    0F
00001F78  E310 5010 0014                 00000010  1351+          LGF   R1,V2ADDR          load v2 source
00001F7E  E761 0000 0806                 00000000  1352+          VL    v22,0(R1)          use v22 to test decoder
00001F84  E766 0000 0C52                           1353+          VCTZ  V22,V22,0          test instruction (dest is a source)
00001F8A  E760 5028 080E                 00001F60  1354+          VST   V22,V1O30          save v1 output
00001F90  07FB                                     1355+          BR    R11                return
00001F94                                           1356+RE30      DC    0F                 xl16 expected result
00001F94                                           1357+          DROP  R5
00001F94  08000304 08000601                        1358           DC    XL16'08000304080006010800020508000502'   expected result
00001F9C  08000205 08000502
00001FA4  00FF0810 00FF4002                        1359           DC    XL16'00FF081000FF400200FF042000FF2004'   v2
00001FAC  00FF0420 00FF2004
                                                   1360
                                                   1361 * Halfword
                                                   1362           VRR_A VCTZ,1
00001FB8                                           1363+          DS    0FD
00001FB8                         00001FB8          1364+          USING *,R5               base for test data and test routine
00001FB8  00001FF8                                 1365+T31       DC    A(X31)             address of test routine
00001FBC  001F                                     1366+          DC    H'31'              test number
00001FBE  00                                       1367+          DC    X'00'
00001FBF  01                                       1368+          DC    HL1'1'             M3
00001FC0  E5C3E3E9 40404040                        1369+          DC    CL8'VCTZ'          instruction name
00001FC8  00002024                                 1370+          DC    A(RE31+16)         address of v2 source
00001FCC  00000010                                 1371+          DC    A(16)              result length
00001FD0  00002014                                 1372+REA31     DC    A(RE31)            result address
00001FD8  00000000 00000000                        1373+          DS    FD                 gap
00001FE0  00000000 00000000                        1374+V1O31     DS    XL16               V1 output
00001FE8  00000000 00000000
00001FF0  00000000 00000000                        1375+          DS    FD                 gap
                                                   1376+*
00001FF8                                           1377+X31       DS    0F
00001FF8  E310 5010 0014                 00000010  1378+          LGF   R1,V2ADDR          load v2 source
00001FFE  E761 0000 0806                 00000000  1379+          VL    v22,0(R1)          use v22 to test decoder
00002004  E766 0000 1C52                           1380+          VCTZ  V22,V22,1          test instruction (dest is a source)
0000200A  E760 5028 080E                 00001FE0  1381+          VST   V22,V1O31          save v1 output
00002010  07FB                                     1382+          BR    R11                return
00002014                                           1383+RE31      DC    0F                 xl16 expected result
00002014                                           1384+          DROP  R5
00002014  00100000 00070008                        1385           DC    XL16'00100000000700080010000000A0005'   expected result
0000201C  00100000 000A0005
00002024  0000FFFF 00800100                        1386           DC    XL16'0000FFFF008001000000FFFF04000020'   v2
0000202C  0000FFFF 04000020
                                                   1387
                                                   1388 * Word
                                                   1389           VRR_A VCTZ,2
00002038                                           1390+          DS    0FD
00002038                         00002038          1391+          USING *,R5               base for test data and test routine
00002038  00002078                                 1392+T32       DC    A(X32)             address of test routine
0000203C  0020                                     1393+          DC    H'32'              test number
0000203E  00                                       1394+          DC    X'00'
0000203F  02                                       1395+          DC    HL1'2'             M3
00002040  E5C3E3E9 40404040                        1396+          DC    CL8'VCTZ'          instruction name
00002048  000020A4                                 1397+          DC    A(RE32+16)         address of v2 source
0000204C  00000010                                 1398+          DC    A(16)              result length
00002050  00002094                                 1399+REA32     DC    A(RE32)            result address
00002058  00000000 00000000                        1400+          DS    FD                 gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002060  00000000 00000000                        1401+V1O32    DS    XL16               V1 output
00002068  00000000 00000000
00002070  00000000 00000000                        1402+         DS    FD                 gap
                                                   1403+*
00002078                                           1404+X32      DS    0F
00002078  E310 5010 0014                 00000010  1405+         LGF   R1,V2ADDR          load v2 source
0000207E  E761 0000 0806                 00000000  1406+         VL    v22,0(R1)          use v22 to test decoder
00002084  E766 0000 2C52                           1407+         VCTZ  V22,V22,2          test instruction (dest is a source)
0000208A  E760 5028 080E                 00002060  1408+         VST   V22,V1O32          save v1 output
00002090  07FB                                     1409+         BR    R11                return
00002094                                           1410+RE32     DC    0F                 xl16 expected result
00002094                                           1411+         DROP  R5
00002094  00000020 00000000                        1412          DC    XL16'00000020000000000000000F00000010'   expected result
0000209C  0000000F 00000010
000020A4  00000000 FFFFFFFF                        1413          DC    XL16'00000000FFFFFFFF0000800000010000'   v2
000020AC  00008000 00010000
                                                   1414
                                                   1415 * Doubleword
                                                   1416          VRR_A VCTZ,3
000020B8                                           1417+         DS    0FD
000020B8                         000020B8          1418+         USING *,R5               base for test data and test routine
000020B8  000020F8                                 1419+T33      DC    A(X33)             address of test routine
000020BC  0021                                     1420+         DC    H'33'              test number
000020BE  00                                       1421+         DC    X'00'
000020BF  03                                       1422+         DC    HL1'3'             M3
000020C0  E5C3E3E9 40404040                        1423+         DC    CL8'VCTZ'          instruction name
000020C8  00002124                                 1424+         DC    A(RE33+16)         address of v2 source
000020CC  00000010                                 1425+         DC    A(16)              result length
000020D0  00002114                                 1426+REA33    DC    A(RE33)            result address
000020D8  00000000 00000000                        1427+         DS    FD                 gap
000020E0  00000000 00000000                        1428+V1O33    DS    XL16               V1 output
000020E8  00000000 00000000
000020F0  00000000 00000000                        1429+         DS    FD                 gap
                                                   1430+*
000020F8                                           1431+X33      DS    0F
000020F8  E310 5010 0014                 00000010  1432+         LGF   R1,V2ADDR          load v2 source
000020FE  E761 0000 0806                 00000000  1433+         VL    v22,0(R1)          use v22 to test decoder
00002104  E766 0000 3C52                           1434+         VCTZ  V22,V22,3          test instruction (dest is a source)
0000210A  E760 5028 080E                 000020E0  1435+         VST   V22,V1O33          save v1 output
00002110  07FB                                     1436+         BR    R11                return
00002114                                           1437+RE33     DC    0F                 xl16 expected result
00002114                                           1438+         DROP  R5
00002114  00000000 00000040                        1439          DC    XL16'00000000000000400000000000000000'   expected result
0000211C  00000000 00000000
00002124  00000000 00000000                        1440          DC    XL16'0000000000000000FFFFFFFFFFFFFFFF'   v2
0000212C  FFFFFFFF FFFFFFFF
                                                   1441
                                                   1442 * Doubleword
                                                   1443          VRR_A VCTZ,3
00002138                                           1444+         DS    0FD
00002138                         00002138          1445+         USING *,R5               base for test data and test routine
00002138  00002178                                 1446+T34      DC    A(X34)             address of test routine
0000213C  0022                                     1447+         DC    H'34'              test number
0000213E  00                                       1448+         DC    X'00'
0000213F  03                                       1449+         DC    HL1'3'             M3
00002140  E5C3E3E9 40404040                        1450+         DC    CL8'VCTZ'          instruction name
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
00002148  000021A4                                  1451+          DC    A(RE34+16)          address of v2 source
0000214C  00000010                                  1452+          DC    A(16)               result length
00002150  00002194                                  1453+REA34     DC    A(RE34)             result address
00002158  00000000 00000000                         1454+          DS    FD                  gap
00002160  00000000 00000000                         1455+V1O34     DS    XL16                V1 output
00002168  00000000 00000000
00002170  00000000 00000000                         1456+          DS    FD                  gap
                                                    1457+*
00002178                                            1458+X34       DS    0F
00002178  E310 5010 0014                 00000010   1459+          LGF   R1,V2ADDR           load v2 source
0000217E  E761 0000 0806                 00000000   1460+          VL    v22,0(R1)           use v22 to test decoder
00002184  E766 0000 3C52                            1461+          VCTZ  V22,V22,3           test instruction (dest is a source)
0000218A  E760 5028 080E                 00002160   1462+          VST   V22,V1O34           save v1 output
00002190  07FB                                      1463+          BR    R11                 return
00002194                                            1464+RE34      DC    0F                  xl16 expected result
00002194                                            1465+          DROP  R5
00002194  00000000 00000017                         1466           DC    XL16'00000000000000170000000000000018'   expected result
0000219C  00000000 00000018
000021A4  00000000 00800000                         1467           DC    XL16'00000000080000000000000001000000'   v2
000021AC  00000000 01000000
                                                    1468
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    1470 *===============================================================================
                                                    1471 *-------------------------------------------------------------------------------
                                                    1472 * VCLZ   - Vector Count Leading Zeros
                                                    1473 *-------------------------------------------------------------------------------
                                                    1474
                                                    1475 *-------------------------------------------------------------------------------
                                                    1476 * case 0 - simple, simple debug
                                                    1477 *-------------------------------------------------------------------------------
                                                    1478 * Byte
                                                    1479          VRR_A VCLZ,0
000021B8                                            1480+         DS    0FD
000021B8                      000021B8              1481+         USING *,R5              base for test data and test routine
000021B8  000021F8                                  1482+T35      DC    A(X35)            address of test routine
000021BC  0023                                      1483+         DC    H'35'             test number
000021BE  00                                        1484+         DC    X'00'
000021BF  00                                        1485+         DC    HL1'0'            M3
000021C0  E5C3D3E9 40404040                         1486+         DC    CL8'VCLZ'         instruction name
000021C8  00002224                                  1487+         DC    A(RE35+16)        address of v2 source
000021CC  00000010                                  1488+         DC    A(16)             result length
000021D0  00002214                                  1489+REA35    DC    A(RE35)           result address
000021D8  00000000 00000000                         1490+         DS    FD                gap
000021E0  00000000 00000000                         1491+V1O35    DS    XL16              V1 output
000021E8  00000000 00000000
000021F0  00000000 00000000                         1492+         DS    FD                gap
                                                    1493+*
000021F8                                            1494+X35      DS    0F
000021F8  E310 5010 0014                 00000010   1495+         LGF   R1,V2ADDR         load v2 source
000021FE  E761 0000 0806                 00000000   1496+         VL    v22,0(R1)         use v22 to test decoder
00002204  E766 0000 0C53                            1497+         VCLZ  V22,V22,0         test instruction (dest is a source)
0000220A  E760 5028 080E                 000021E0   1498+         VST   V22,V1O35         save v1 output
00002210  07FB                                      1499+         BR    R11               return
00002214                                            1500+RE35     DC    0F                xl16 expected result
00002214                                            1501+         DROP  R5
00002214  08080808 08080808                         1502          DC    XL16'08080808080808080808080808080808'   expected result
0000221C  08080808 08080808
00002224  00000000 00000000                         1503          DC    XL16'00000000000000000000000000000000'   v2
0000222C  00000000 00000000
                                                    1504
                                                    1505 * Halfword
                                                    1506          VRR_A VCLZ,1
00002238                                            1507+         DS    0FD
00002238                      00002238              1508+         USING *,R5              base for test data and test routine
00002238  00002278                                  1509+T36      DC    A(X36)            address of test routine
0000223C  0024                                      1510+         DC    H'36'             test number
0000223E  00                                        1511+         DC    X'00'
0000223F  01                                        1512+         DC    HL1'1'            M3
00002240  E5C3D3E9 40404040                         1513+         DC    CL8'VCLZ'         instruction name
00002248  000022A4                                  1514+         DC    A(RE36+16)        address of v2 source
0000224C  00000010                                  1515+         DC    A(16)             result length
00002250  00002294                                  1516+REA36    DC    A(RE36)           result address
00002258  00000000 00000000                         1517+         DS    FD                gap
00002260  00000000 00000000                         1518+V1O36    DS    XL16              V1 output
00002268  00000000 00000000
00002270  00000000 00000000                         1519+         DS    FD                gap
                                                    1520+*
00002278                                            1521+X36      DS    0F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002278  E310 5010 0014                 00000010  1522+          LGF   R1,V2ADDR          load v2 source
0000227E  E761 0000 0806                 00000000  1523+          VL    v22,0(R1)          use v22 to test decoder
00002284  E766 0000 1C53                           1524+          VCLZ  V22,V22,1          test instruction (dest is a source)
0000228A  E760 5028 080E                 00002260  1525+          VST   V22,V1O36          save v1 output
00002290  07FB                                     1526+          BR    R11                return
00002294                                           1527+RE36      DC    0F                 xl16 expected result
00002294                                           1528+          DROP  R5
00002294  00100010 00100010                        1529           DC    XL16'00100010001000100010001000100010'   expected result
0000229C  00100010 00100010
000022A4  00000000 00000000                        1530           DC    XL16'00000000000000000000000000000000'   v2
000022AC  00000000 00000000
                                                   1531
                                                   1532 * Word
                                                   1533           VRR_A VCLZ,2
000022B8                                           1534+          DS    0FD
000022B8                         000022B8          1535+          USING *,R5               base for test data and test routine
000022B8  000022F8                                 1536+T37       DC    A(X37)             address of test routine
000022BC  0025                                     1537+          DC    H'37'              test number
000022BE  00                                       1538+          DC    X'00'
000022BF  02                                       1539+          DC    HL1'2'             M3
000022C0  E5C3D3E9 40404040                        1540+          DC    CL8'VCLZ'          instruction name
000022C8  00002324                                 1541+          DC    A(RE37+16)         address of v2 source
000022CC  00000010                                 1542+          DC    A(16)              result length
000022D0  00002314                                 1543+REA37     DC    A(RE37)            result address
000022D8  00000000 00000000                        1544+          DS    FD                 gap
000022E0  00000000 00000000                        1545+V1O37     DS    XL16               V1 output
000022E8  00000000 00000000
000022F0  00000000 00000000                        1546+          DS    FD                 gap
                                                   1547+*
000022F8                                           1548+X37       DS    0F
000022F8  E310 5010 0014                 00000010  1549+          LGF   R1,V2ADDR          load v2 source
000022FE  E761 0000 0806                 00000000  1550+          VL    v22,0(R1)          use v22 to test decoder
00002304  E766 0000 2C53                           1551+          VCLZ  V22,V22,2          test instruction (dest is a source)
0000230A  E760 5028 080E                 000022E0  1552+          VST   V22,V1O37          save v1 output
00002310  07FB                                     1553+          BR    R11                return
00002314                                           1554+RE37      DC    0F                 xl16 expected result
00002314                                           1555+          DROP  R5
00002314  00000020 00000020                        1556           DC    XL16'00000020000000200000002000000020'   expected result
0000231C  00000020 00000020
00002324  00000000 00000000                        1557           DC    XL16'00000000000000000000000000000000'   v2
0000232C  00000000 00000000
                                                   1558
                                                   1559 * Doubleword
                                                   1560           VRR_A VCLZ,3
00002338                                           1561+          DS    0FD
00002338                         00002338          1562+          USING *,R5               base for test data and test routine
00002338  00002378                                 1563+T38       DC    A(X38)             address of test routine
0000233C  0026                                     1564+          DC    H'38'              test number
0000233E  00                                       1565+          DC    X'00'
0000233F  03                                       1566+          DC    HL1'3'             M3
00002340  E5C3D3E9 40404040                        1567+          DC    CL8'VCLZ'          instruction name
00002348  000023A4                                 1568+          DC    A(RE38+16)         address of v2 source
0000234C  00000010                                 1569+          DC    A(16)              result length
00002350  00002394                                 1570+REA38     DC    A(RE38)            result address
00002358  00000000 00000000                        1571+          DS    FD                 gap
00002360  00000000 00000000                        1572+V1O38     DS    XL16               V1 output
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002368  00000000 00000000
00002370  00000000 00000000                        1573+         DS    FD                  gap
                                                   1574+*
00002378                                           1575+X38      DS    0F
00002378  E310 5010 0014                 00000010  1576+         LGF   R1,V2ADDR           load v2 source
0000237E  E761 0000 0806                 00000000  1577+         VL    v22,0(R1)           use v22 to test decoder
00002384  E766 0000 3C53                           1578+         VCLZ  V22,V22,3           test instruction (dest is a source)
0000238A  E760 5028 080E                 00002360  1579+         VST   V22,V1O38           save v1 output
00002390  07FB                                     1580+         BR    R11                 return
00002394                                           1581+RE38     DC    0F                  xl16 expected result
00002394                                           1582+         DROP  R5
00002394  00000000 00000040                        1583          DC    XL16'00000000000000400000000000000040'   expected result
0000239C  00000000 00000040
000023A4  00000000 00000000                        1584          DC    XL16'00000000000000000000000000000000'   v2
000023AC  00000000 00000000
                                                   1585
                                                   1586 *-------------------------------------------------------------------
                                                   1587 * Byte
                                                   1588          VRR_A VCLZ,0
000023B8                                           1589+         DS    0FD
000023B8                          000023B8         1590+         USING *,R5                base for test data and test routine
000023B8  000023F8                                 1591+T39      DC    A(X39)              address of test routine
000023BC  0027                                     1592+         DC    H'39'               test number
000023BE  00                                       1593+         DC    X'00'
000023BF  00                                       1594+         DC    HL1'0'              M3
000023C0  E5C3D3E9 40404040                        1595+         DC    CL8'VCLZ'           instruction name
000023C8  00002424                                 1596+         DC    A(RE39+16)          address of v2 source
000023CC  00000010                                 1597+         DC    A(16)               result length
000023D0  00002414                                 1598+REA39    DC    A(RE39)             result address
000023D8  00000000 00000000                        1599+         DS    FD                  gap
000023E0  00000000 00000000                        1600+V1O39    DS    XL16                V1 output
000023E8  00000000 00000000
000023F0  00000000 00000000                        1601+         DS    FD                  gap
                                                   1602+*
000023F8                                           1603+X39      DS    0F
000023F8  E310 5010 0014                 00000010  1604+         LGF   R1,V2ADDR           load v2 source
000023FE  E761 0000 0806                 00000000  1605+         VL    v22,0(R1)           use v22 to test decoder
00002404  E766 0000 0C53                           1606+         VCLZ  V22,V22,0           test instruction (dest is a source)
0000240A  E760 5028 080E                 000023E0  1607+         VST   V22,V1O39           save v1 output
00002410  07FB                                     1608+         BR    R11                 return
00002414                                           1609+RE39     DC    0F                  xl16 expected result
00002414                                           1610+         DROP  R5
00002414  00000000 00000000                        1611          DC    XL16'00000000000000000000000000000000'   expected result
0000241C  00000000 00000000
00002424  FFFFFFFF FFFFFFFF                        1612          DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'   v2
0000242C  FFFFFFFF FFFFFFFF
                                                   1613
                                                   1614 * Halfword
                                                   1615          VRR_A VCLZ,1
00002438                                           1616+         DS    0FD
00002438                          00002438         1617+         USING *,R5                base for test data and test routine
00002438  00002478                                 1618+T40      DC    A(X40)              address of test routine
0000243C  0028                                     1619+         DC    H'40'               test number
0000243E  00                                       1620+         DC    X'00'
0000243F  01                                       1621+         DC    HL1'1'              M3
00002440  E5C3D3E9 40404040                        1622+         DC    CL8'VCLZ'           instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002448  000024A4                                1623+          DC    A(RE40+16)          address of v2 source
0000244C  00000010                                1624+          DC    A(16)               result length
00002450  00002494                                1625+REA40     DC    A(RE40)             result address
00002458  00000000 00000000                       1626+          DS    FD                  gap
00002460  00000000 00000000                       1627+V1O40     DS    XL16                V1 output
00002468  00000000 00000000
00002470  00000000 00000000                       1628+          DS    FD                  gap
                                                  1629+*
00002478                                          1630+X40       DS    0F
00002478  E310 5010 0014                 00000010 1631+          LGF   R1,V2ADDR           load v2 source
0000247E  E761 0000 0806                 00000000 1632+          VL    v22,0(R1)           use v22 to test decoder
00002484  E766 0000 1C53                          1633+          VCLZ  V22,V22,1           test instruction (dest is a source)
0000248A  E760 5028 080E                 00002460 1634+          VST   V22,V1O40           save v1 output
00002490  07FB                                    1635+          BR    R11                 return
00002494                                          1636+RE40      DC    0F                  xl16 expected result
00002494                                          1637+          DROP  R5
00002494  00000000 00000000                       1638           DC    XL16'00000000000000000000000000000000'   expected result
0000249C  00000000 00000000
000024A4  FFFFFFFF FFFFFFFF                       1639           DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'   v2
000024AC  FFFFFFFF FFFFFFFF
                                                  1640
                                                  1641 * Word
                                                  1642           VRR_A VCLZ,2
000024B8                                          1643+          DS    0FD
000024B8                  000024B8                1644+          USING *,R5                base for test data and test routine
000024B8  000024F8                                1645+T41       DC    A(X41)              address of test routine
000024BC  0029                                    1646+          DC    H'41'               test number
000024BE  00                                      1647+          DC    X'00'
000024BF  02                                      1648+          DC    HL1'2'              M3
000024C0  E5C3D3E9 40404040                       1649+          DC    CL8'VCLZ'           instruction name
000024C8  00002524                                1650+          DC    A(RE41+16)          address of v2 source
000024CC  00000010                                1651+          DC    A(16)               result length
000024D0  00002514                                1652+REA41     DC    A(RE41)             result address
000024D8  00000000 00000000                       1653+          DS    FD                  gap
000024E0  00000000 00000000                       1654+V1O41     DS    XL16                V1 output
000024E8  00000000 00000000
000024F0  00000000 00000000                       1655+          DS    FD                  gap
                                                  1656+*
000024F8                                          1657+X41       DS    0F
000024F8  E310 5010 0014                 00000010 1658+          LGF   R1,V2ADDR           load v2 source
000024FE  E761 0000 0806                 00000000 1659+          VL    v22,0(R1)           use v22 to test decoder
00002504  E766 0000 2C53                          1660+          VCLZ  V22,V22,2           test instruction (dest is a source)
0000250A  E760 5028 080E                 000024E0 1661+          VST   V22,V1O41           save v1 output
00002510  07FB                                    1662+          BR    R11                 return
00002514                                          1663+RE41      DC    0F                  xl16 expected result
00002514                                          1664+          DROP  R5
00002514  00000000 00000000                       1665           DC    XL16'00000000000000000000000000000000'   expected result
0000251C  00000000 00000000
00002524  FFFFFFFF FFFFFFFF                       1666           DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'   v2
0000252C  FFFFFFFF FFFFFFFF
                                                  1667
                                                  1668 * Doubleword
                                                  1669           VRR_A VCLZ,3
00002538                                          1670+          DS    0FD
00002538                  00002538                1671+          USING *,R5                base for test data and test routine
00002538  00002578                                1672+T42       DC    A(X42)              address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
0000253C  002A                                    1673+          DC    H'42'               test number
0000253E  00                                      1674+          DC    X'00'
0000253F  03                                      1675+          DC    HL1'3'              M3
00002540  E5C3D3E9 40404040                       1676+          DC    CL8'VCLZ'           instruction name
00002548  000025A4                                1677+          DC    A(RE42+16)          address of v2 source
0000254C  00000010                                1678+          DC    A(16)               result length
00002550  00002594                                1679+REA42     DC    A(RE42)             result address
00002558  00000000 00000000                       1680+          DS    FD                  gap
00002560  00000000 00000000                       1681+V1O42     DS    XL16                V1 output
00002568  00000000 00000000
00002570  00000000 00000000                       1682+          DS    FD                  gap
                                                  1683+*
00002578                                          1684+X42       DS    0F
00002578  E310 5010 0014                 00000010 1685+          LGF   R1,V2ADDR           load v2 source
0000257E  E761 0000 0806                 00000000 1686+          VL    v22,0(R1)           use v22 to test decoder
00002584  E766 0000 3C53                          1687+          VCLZ  V22,V22,3           test instruction (dest is a source)
0000258A  E760 5028 080E                 00002560 1688+          VST   V22,V1O42           save v1 output
00002590  07FB                                    1689+          BR    R11                 return
00002594                                          1690+RE42      DC    0F                  xl16 expected result
00002594                                          1691+          DROP  R5
00002594  00000000 00000000                       1692           DC    XL16'00000000000000000000000000000000'   expected result
0000259C  00000000 00000000
000025A4  FFFFFFFF FFFFFFFF                       1693           DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'   v2
000025AC  FFFFFFFF FFFFFFFF
                                                  1694
                                                  1695 *-------------------------------------------------------------------
                                                  1696 * case 1 - simple
                                                  1697 *-------------------------------------------------------------------
                                                  1698 * Byte
                                                  1699           VRR_A VCLZ,0
000025B8                                          1700+          DS    0FD
000025B8                      000025B8            1701+          USING *,R5                base for test data and test routine
000025B8  000025F8                                1702+T43       DC    A(X43)              address of test routine
000025BC  002B                                    1703+          DC    H'43'               test number
000025BE  00                                      1704+          DC    X'00'
000025BF  00                                      1705+          DC    HL1'0'              M3
000025C0  E5C3D3E9 40404040                       1706+          DC    CL8'VCLZ'           instruction name
000025C8  00002624                                1707+          DC    A(RE43+16)          address of v2 source
000025CC  00000010                                1708+          DC    A(16)               result length
000025D0  00002614                                1709+REA43     DC    A(RE43)             result address
000025D8  00000000 00000000                       1710+          DS    FD                  gap
000025E0  00000000 00000000                       1711+V1O43     DS    XL16                V1 output
000025E8  00000000 00000000
000025F0  00000000 00000000                       1712+          DS    FD                  gap
                                                  1713+*
000025F8                                          1714+X43       DS    0F
000025F8  E310 5010 0014                 00000010 1715+          LGF   R1,V2ADDR           load v2 source
000025FE  E761 0000 0806                 00000000 1716+          VL    v22,0(R1)           use v22 to test decoder
00002604  E766 0000 0C53                          1717+          VCLZ  V22,V22,0           test instruction (dest is a source)
0000260A  E760 5028 080E                 000025E0 1718+          VST   V22,V1O43           save v1 output
00002610  07FB                                    1719+          BR    R11                 return
00002614                                          1720+RE43      DC    0F                  xl16 expected result
00002614                                          1721+          DROP  R5
00002614  08070606 05050505                       1722           DC    XL16'08070606050505050404040404040404'   expected result
0000261C  04040404 04040404
00002624  00010203 04050607                       1723           DC    XL16'000102030405060708090A0B0C0D0E0F'   v2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
0000262C  08090A0B 0C0D0E0F                          1724
                                                     1725 * Halfword
                                                     1726          VRR_A VCLZ,1
00002638                                             1727+         DS    0FD
00002638                      00002638               1728+         USING *,R5              base for test data and test routine
00002638  00002678                                   1729+T44      DC    A(X44)            address of test routine
0000263C  002C                                       1730+         DC    H'44'             test number
0000263E  00                                         1731+         DC    X'00'
0000263F  01                                         1732+         DC    HL1'1'            M3
00002640  E5C3D3E9 40404040                          1733+         DC    CL8'VCLZ'         instruction name
00002648  000026A4                                   1734+         DC    A(RE44+16)        address of v2 source
0000264C  00000010                                   1735+         DC    A(16)             result length
00002650  00002694                                   1736+REA44    DC    A(RE44)           result address
00002658  00000000 00000000                          1737+         DS    FD                gap
00002660  00000000 00000000                          1738+V1O44    DS    XL16              V1 output
00002668  00000000 00000000
00002670  00000000 00000000                          1739+         DS    FD                gap
                                                     1740+*
00002678                                             1741+X44      DS    0F
00002678  E310 5010 0014                00000010     1742+         LGF   R1,V2ADDR         load v2 source
0000267E  E761 0000 0806                00000000     1743+         VL    v22,0(R1)         use v22 to test decoder
00002684  E766 0000 1C53                             1744+         VCLZ  V22,V22,1         test instruction (dest is a source)
0000268A  E760 5028 080E                00002660     1745+         VST   V22,V1O44         save v1 output
00002690  07FB                                       1746+         BR    R11               return
00002694                                             1747+RE44     DC    0F                xl16 expected result
00002694                                             1748+         DROP  R5
00002694  00000000 0009000B                          1749          DC    XL16'00000000009000B000A0004000C0004'   expected result
0000269C  000A0004 000C0004
000026A4  BDEFADEF 005F001F                          1750          DC    XL16'BDEFADEF005F001F003F088F000F0DEF'   v2
000026AC  003F088F 000F0DEF
                                                     1751
                                                     1752 * Word
                                                     1753          VRR_A VCLZ,2
000026B8                                             1754+         DS    0FD
000026B8                      000026B8               1755+         USING *,R5              base for test data and test routine
000026B8  000026F8                                   1756+T45      DC    A(X45)            address of test routine
000026BC  002D                                       1757+         DC    H'45'             test number
000026BE  00                                         1758+         DC    X'00'
000026BF  02                                         1759+         DC    HL1'2'            M3
000026C0  E5C3D3E9 40404040                          1760+         DC    CL8'VCLZ'         instruction name
000026C8  00002724                                   1761+         DC    A(RE45+16)        address of v2 source
000026CC  00000010                                   1762+         DC    A(16)             result length
000026D0  00002714                                   1763+REA45    DC    A(RE45)           result address
000026D8  00000000 00000000                          1764+         DS    FD                gap
000026E0  00000000 00000000                          1765+V1O45    DS    XL16              V1 output
000026E8  00000000 00000000
000026F0  00000000 00000000                          1766+         DS    FD                gap
                                                     1767+*
000026F8                                             1768+X45      DS    0F
000026F8  E310 5010 0014                00000010     1769+         LGF   R1,V2ADDR         load v2 source
000026FE  E761 0000 0806                00000000     1770+         VL    v22,0(R1)         use v22 to test decoder
00002704  E766 0000 2C53                             1771+         VCLZ  V22,V22,2         test instruction (dest is a source)
0000270A  E760 5028 080E                000026E0     1772+         VST   V22,V1O45         save v1 output
00002710  07FB                                       1773+         BR    R11               return
00002714                                             1774+RE45     DC    0F                xl16 expected result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002714                                           1775+         DROP  R5
00002714  00000000 00000009                        1776          DC    XL16'0000000000000009000000A0000000C'   expected result
0000271C  0000000A 0000000C
00002724  BDEFADEF 005F001F                        1777          DC    XL16'BDEFADEF005F001F003F088F000F0DEF'   v2
0000272C  003F088F 000F0DEF
                                                   1778
                                                   1779 * Doubleword
                                                   1780          VRR_A VCLZ,3
00002738                                           1781+         DS    0FD
00002738                    00002738               1782+         USING *,R5              base for test data and test routine
00002738  00002778                                 1783+T46      DC    A(X46)            address of test routine
0000273C  002E                                     1784+         DC    H'46'             test number
0000273E  00                                       1785+         DC    X'00'
0000273F  03                                       1786+         DC    HL1'3'            M3
00002740  E5C3D3E9 40404040                        1787+         DC    CL8'VCLZ'         instruction name
00002748  000027A4                                 1788+         DC    A(RE46+16)        address of v2 source
0000274C  00000010                                 1789+         DC    A(16)             result length
00002750  00002794                                 1790+REA46    DC    A(RE46)           result address
00002758  00000000 00000000                        1791+         DS    FD                gap
00002760  00000000 00000000                        1792+V1O46    DS    XL16              V1 output
00002768  00000000 00000000
00002770  00000000 00000000                        1793+         DS    FD                gap
                                                   1794+*
00002778                                           1795+X46      DS    0F
00002778  E310 5010 0014                00000010   1796+         LGF   R1,V2ADDR         load v2 source
0000277E  E761 0000 0806                00000000   1797+         VL    v22,0(R1)         use v22 to test decoder
00002784  E766 0000 3C53                           1798+         VCLZ  V22,V22,3         test instruction (dest is a source)
0000278A  E760 5028 080E                00002760   1799+         VST   V22,V1O46         save v1 output
00002790  07FB                                     1800+         BR    R11               return
00002794                                           1801+RE46     DC    0F                xl16 expected result
00002794                                           1802+         DROP  R5
00002794  00000000 00000000                        1803          DC    XL16'0000000000000000000000000000000A'   expected result
0000279C  00000000 0000000A
000027A4  BDEFADEF 005F001F                        1804          DC    XL16'BDEFADEF005F001F003F088F000F0DEF'   v2
000027AC  003F088F 000F0DEF
                                                   1805
                                                   1806 *-------------------------------------------------------------------
                                                   1807 * case 2 - hw verified
                                                   1808 *-------------------------------------------------------------------
                                                   1809 * Byte
                                                   1810          VRR_A VCLZ,0
000027B8                                           1811+         DS    0FD
000027B8                    000027B8               1812+         USING *,R5              base for test data and test routine
000027B8  000027F8                                 1813+T47      DC    A(X47)            address of test routine
000027BC  002F                                     1814+         DC    H'47'             test number
000027BE  00                                       1815+         DC    X'00'
000027BF  00                                       1816+         DC    HL1'0'            M3
000027C0  E5C3D3E9 40404040                        1817+         DC    CL8'VCLZ'         instruction name
000027C8  00002824                                 1818+         DC    A(RE47+16)        address of v2 source
000027CC  00000010                                 1819+         DC    A(16)             result length
000027D0  00002814                                 1820+REA47    DC    A(RE47)           result address
000027D8  00000000 00000000                        1821+         DS    FD                gap
000027E0  00000000 00000000                        1822+V1O47    DS    XL16              V1 output
000027E8  00000000 00000000
000027F0  00000000 00000000                        1823+         DS    FD                gap
                                                   1824+*
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000027F8                                          1825+X47      DS    0F
000027F8  E310 5010 0014                 00000010 1826+         LGF   R1,V2ADDR          load v2 source
000027FE  E761 0000 0806                 00000000 1827+         VL    v22,0(R1)          use v22 to test decoder
00002804  E766 0000 0C53                          1828+         VCLZ  V22,V22,0          test instruction (dest is a source)
0000280A  E760 5028 080E                 000027E0 1829+         VST   V22,V1O47          save v1 output
00002810  07FB                                    1830+         BR    R11                return
00002814                                          1831+RE47     DC    0F                 xl16 expected result
00002814                                          1832+         DROP  R5
00002814  08000403 08000106                       1833          DC    XL16'08000403080001060800050208000205'   expected result
0000281C  08000502 08000205
00002824  00FF0810 00FF4002                       1834          DC    XL16'00FF081000FF400200FF042000FF2004'   v2
0000282C  00FF0420 00FF2004
                                                  1835
                                                  1836 * Halfword
                                                  1837          VRR_A VCLZ,1
00002838                                          1838+         DS    0FD
00002838                         00002838         1839+         USING *,R5               base for test data and test routine
00002838  00002878                                1840+T48      DC    A(X48)             address of test routine
0000283C  0030                                    1841+         DC    H'48'              test number
0000283E  00                                      1842+         DC    X'00'
0000283F  01                                      1843+         DC    HL1'1'             M3
00002840  E5C3D3E9 40404040                       1844+         DC    CL8'VCLZ'          instruction name
00002848  000028A4                                1845+         DC    A(RE48+16)         address of v2 source
0000284C  00000010                                1846+         DC    A(16)              result length
00002850  00002894                                1847+REA48    DC    A(RE48)            result address
00002858  00000000 00000000                       1848+         DS    FD                 gap
00002860  00000000 00000000                       1849+V1O48    DS    XL16               V1 output
00002868  00000000 00000000
00002870  00000000 00000000                       1850+         DS    FD                 gap
                                                  1851+*
00002878                                          1852+X48      DS    0F
00002878  E310 5010 0014                 00000010 1853+         LGF   R1,V2ADDR          load v2 source
0000287E  E761 0000 0806                 00000000 1854+         VL    v22,0(R1)          use v22 to test decoder
00002884  E766 0000 1C53                          1855+         VCLZ  V22,V22,1          test instruction (dest is a source)
0000288A  E760 5028 080E                 00002860 1856+         VST   V22,V1O48          save v1 output
00002890  07FB                                    1857+         BR    R11                return
00002894                                          1858+RE48     DC    0F                 xl16 expected result
00002894                                          1859+         DROP  R5
00002894  00100000 00080007                       1860          DC    XL16'00100000000800070010000000005000A'   expected result
0000289C  00100000 0005000A
000028A4  0000FFFF 00800100                       1861          DC    XL16'0000FFFF008001000000FFFF04000020'   v2
000028AC  0000FFFF 04000020
                                                  1862
                                                  1863 * Word
                                                  1864          VRR_A VCLZ,2
000028B8                                          1865+         DS    0FD
000028B8                         000028B8         1866+         USING *,R5               base for test data and test routine
000028B8  000028F8                                1867+T49      DC    A(X49)             address of test routine
000028BC  0031                                    1868+         DC    H'49'              test number
000028BE  00                                      1869+         DC    X'00'
000028BF  02                                      1870+         DC    HL1'2'             M3
000028C0  E5C3D3E9 40404040                       1871+         DC    CL8'VCLZ'          instruction name
000028C8  00002924                                1872+         DC    A(RE49+16)         address of v2 source
000028CC  00000010                                1873+         DC    A(16)              result length
000028D0  00002914                                1874+REA49    DC    A(RE49)            result address
000028D8  00000000 00000000                       1875+         DS    FD                 gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000028E0  00000000 00000000                      1876+V1O49    DS    XL16               V1 output
000028E8  00000000 00000000
000028F0  00000000 00000000                      1877+         DS    FD                 gap
                                                 1878+*
000028F8                                         1879+X49      DS    0F
000028F8  E310 5010 0014                00000010 1880+         LGF   R1,V2ADDR          load v2 source
000028FE  E761 0000 0806                00000000 1881+         VL    v22,0(R1)          use v22 to test decoder
00002904  E766 0000 2C53                         1882+         VCLZ  V22,V22,2          test instruction (dest is a source)
0000290A  E760 5028 080E                000028E0 1883+         VST   V22,V1O49          save v1 output
00002910  07FB                                   1884+         BR    R11                return
00002914                                         1885+RE49     DC    0F                 xl16 expected result
00002914                                         1886+         DROP  R5
00002914  00000020 00000000                      1887          DC    XL16'00000020000000000000000100000000F'   expected result
0000291C  00000010 0000000F
00002924  00000000 FFFFFFFF                      1888          DC    XL16'00000000FFFFFFFF0000800000010000'   v2
0000292C  00008000 00010000
                                                 1889
                                                 1890 * Doubleword
                                                 1891          VRR_A VCLZ,3
00002938                                         1892+         DS    0FD
00002938                  00002938               1893+         USING *,R5               base for test data and test routine
00002938  00002978                               1894+T50      DC    A(X50)             address of test routine
0000293C  0032                                   1895+         DC    H'50'              test number
0000293E  00                                     1896+         DC    X'00'
0000293F  03                                     1897+         DC    HL1'3'             M3
00002940  E5C3D3E9 40404040                      1898+         DC    CL8'VCLZ'          instruction name
00002948  000029A4                               1899+         DC    A(RE50+16)         address of v2 source
0000294C  00000010                               1900+         DC    A(16)              result length
00002950  00002994                               1901+REA50    DC    A(RE50)            result address
00002958  00000000 00000000                      1902+         DS    FD                 gap
00002960  00000000 00000000                      1903+V1O50    DS    XL16               V1 output
00002968  00000000 00000000
00002970  00000000 00000000                      1904+         DS    FD                 gap
                                                 1905+*
00002978                                         1906+X50      DS    0F
00002978  E310 5010 0014                00000010 1907+         LGF   R1,V2ADDR          load v2 source
0000297E  E761 0000 0806                00000000 1908+         VL    v22,0(R1)          use v22 to test decoder
00002984  E766 0000 3C53                         1909+         VCLZ  V22,V22,3          test instruction (dest is a source)
0000298A  E760 5028 080E                00002960 1910+         VST   V22,V1O50          save v1 output
00002990  07FB                                   1911+         BR    R11                return
00002994                                         1912+RE50     DC    0F                 xl16 expected result
00002994                                         1913+         DROP  R5
00002994  00000000 00000040                      1914          DC    XL16'00000000000000400000000000000000'   expected result
0000299C  00000000 00000000
000029A4  00000000 00000000                      1915          DC    XL16'0000000000000000FFFFFFFFFFFFFFFF'   v2
000029AC  FFFFFFFF FFFFFFFF
                                                 1916
                                                 1917 * Doubleword
                                                 1918          VRR_A VCLZ,3
000029B8                                         1919+         DS    0FD
000029B8                  000029B8               1920+         USING *,R5               base for test data and test routine
000029B8  000029F8                               1921+T51      DC    A(X51)             address of test routine
000029BC  0033                                   1922+         DC    H'51'              test number
000029BE  00                                     1923+         DC    X'00'
000029BF  03                                     1924+         DC    HL1'3'             M3
000029C0  E5C3D3E9 40404040                      1925+         DC    CL8'VCLZ'          instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000029C8  00002A24                                1926+          DC    A(RE51+16)          address of v2 source
000029CC  00000010                                1927+          DC    A(16)               result length
000029D0  00002A14                                1928+REA51     DC    A(RE51)             result address
000029D8  00000000 00000000                       1929+          DS    FD                  gap
000029E0  00000000 00000000                       1930+V1O51     DS    XL16                V1 output
000029E8  00000000 00000000
000029F0  00000000 00000000                       1931+          DS    FD                  gap
                                                  1932+*
000029F8                                          1933+X51       DS    0F
000029F8  E310 5010 0014                 00000010 1934+          LGF   R1,V2ADDR           load v2 source
000029FE  E761 0000 0806                 00000000 1935+          VL    v22,0(R1)           use v22 to test decoder
00002A04  E766 0000 3C53                          1936+          VCLZ  V22,V22,3           test instruction (dest is a source)
00002A0A  E760 5028 080E                 000029E0 1937+          VST   V22,V1O51           save v1 output
00002A10  07FB                                    1938+          BR    R11                 return
00002A14                                          1939+RE51      DC    0F                  xl16 expected result
00002A14                                          1940+          DROP  R5
00002A14  00000000 00000028                       1941           DC    XL16'00000000000000280000000000000027'   expected result
00002A1C  00000000 00000027
00002A24  00000000 00800000                       1942           DC    XL16'00000000080000000000000001000000'   v2
00002A2C  00000000 01000000
                                                  1943
                                                  1944
00002A34  00000000                                1945           DC    F'0'     END OF TABLE
00002A38  00000000                                1946           DC    F'0'
                                                  1947 *
                                                  1948 * table of pointers to individual load test
                                                  1949 *
00002A3C                                          1950 E7TESTS   DS    0F
                                                  1951           PTTABLE
00002A3C                                          1952+TTABLE    DS    0F
00002A3C  000010B8                                1953+          DC    A(T1)                    TEST &CUR
00002A40  00001138                                1954+          DC    A(T2)                    TEST &CUR
00002A44  000011B8                                1955+          DC    A(T3)                    TEST &CUR
00002A48  00001238                                1956+          DC    A(T4)                    TEST &CUR
00002A4C  000012B8                                1957+          DC    A(T5)                    TEST &CUR
00002A50  00001338                                1958+          DC    A(T6)                    TEST &CUR
00002A54  000013B8                                1959+          DC    A(T7)                    TEST &CUR
00002A58  00001438                                1960+          DC    A(T8)                    TEST &CUR
00002A5C  000014B8                                1961+          DC    A(T9)                    TEST &CUR
00002A60  00001538                                1962+          DC    A(T10)                   TEST &CUR
00002A64  000015B8                                1963+          DC    A(T11)                   TEST &CUR
00002A68  00001638                                1964+          DC    A(T12)                   TEST &CUR
00002A6C  000016B8                                1965+          DC    A(T13)                   TEST &CUR
00002A70  00001738                                1966+          DC    A(T14)                   TEST &CUR
00002A74  000017B8                                1967+          DC    A(T15)                   TEST &CUR
00002A78  00001838                                1968+          DC    A(T16)                   TEST &CUR
00002A7C  000018B8                                1969+          DC    A(T17)                   TEST &CUR
00002A80  00001938                                1970+          DC    A(T18)                   TEST &CUR
00002A84  000019B8                                1971+          DC    A(T19)                   TEST &CUR
00002A88  00001A38                                1972+          DC    A(T20)                   TEST &CUR
00002A8C  00001AB8                                1973+          DC    A(T21)                   TEST &CUR
00002A90  00001B38                                1974+          DC    A(T22)                   TEST &CUR
00002A94  00001BB8                                1975+          DC    A(T23)                   TEST &CUR
00002A98  00001C38                                1976+          DC    A(T24)                   TEST &CUR
00002A9C  00001CB8                                1977+          DC    A(T25)                   TEST &CUR
00002AA0  00001D38                                1978+          DC    A(T26)                   TEST &CUR
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002AA4  00001DB8                          1979+          DC    A(T27)                  TEST &CUR
00002AA8  00001E38                          1980+          DC    A(T28)                  TEST &CUR
00002AAC  00001EB8                          1981+          DC    A(T29)                  TEST &CUR
00002AB0  00001F38                          1982+          DC    A(T30)                  TEST &CUR
00002AB4  00001FB8                          1983+          DC    A(T31)                  TEST &CUR
00002AB8  00002038                          1984+          DC    A(T32)                  TEST &CUR
00002ABC  000020B8                          1985+          DC    A(T33)                  TEST &CUR
00002AC0  00002138                          1986+          DC    A(T34)                  TEST &CUR
00002AC4  000021B8                          1987+          DC    A(T35)                  TEST &CUR
00002AC8  00002238                          1988+          DC    A(T36)                  TEST &CUR
00002ACC  000022B8                          1989+          DC    A(T37)                  TEST &CUR
00002AD0  00002338                          1990+          DC    A(T38)                  TEST &CUR
00002AD4  000023B8                          1991+          DC    A(T39)                  TEST &CUR
00002AD8  00002438                          1992+          DC    A(T40)                  TEST &CUR
00002ADC  000024B8                          1993+          DC    A(T41)                  TEST &CUR
00002AE0  00002538                          1994+          DC    A(T42)                  TEST &CUR
00002AE4  000025B8                          1995+          DC    A(T43)                  TEST &CUR
00002AE8  00002638                          1996+          DC    A(T44)                  TEST &CUR
00002AEC  000026B8                          1997+          DC    A(T45)                  TEST &CUR
00002AF0  00002738                          1998+          DC    A(T46)                  TEST &CUR
00002AF4  000027B8                          1999+          DC    A(T47)                  TEST &CUR
00002AF8  00002838                          2000+          DC    A(T48)                  TEST &CUR
00002AFC  000028B8                          2001+          DC    A(T49)                  TEST &CUR
00002B00  00002938                          2002+          DC    A(T50)                  TEST &CUR
00002B04  000029B8                          2003+          DC    A(T51)                  TEST &CUR
                                            2004+*
00002B08  00000000                          2005+          DC    A(0)                    END OF TABLE
00002B0C  00000000                          2006+          DC    A(0)                    END OF TABLE
                                            2007
00002B10  00000000                          2008           DC    F'0'     END OF TABLE
00002B14  00000000                          2009           DC    F'0'
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                        2011 ********************************************************************************
                                        2012 *        Register equates
                                        2013 ********************************************************************************


                             00000000  00000001  2015 R0       EQU   0
                             00000001  00000001  2016 R1       EQU   1
                             00000002  00000001  2017 R2       EQU   2
                             00000003  00000001  2018 R3       EQU   3
                             00000004  00000001  2019 R4       EQU   4
                             00000005  00000001  2020 R5       EQU   5
                             00000006  00000001  2021 R6       EQU   6
                             00000007  00000001  2022 R7       EQU   7
                             00000008  00000001  2023 R8       EQU   8
                             00000009  00000001  2024 R9       EQU   9
                             0000000A  00000001  2025 R10      EQU   10
                             0000000B  00000001  2026 R11      EQU   11
                             0000000C  00000001  2027 R12      EQU   12
                             0000000D  00000001  2028 R13      EQU   13
                             0000000E  00000001  2029 R14      EQU   14
                             0000000F  00000001  2030 R15      EQU   15


                                        2032 ********************************************************************************
                                        2033 *        Register equates
                                        2034 ********************************************************************************


                             00000000  00000001  2036 V0       EQU   0
                             00000001  00000001  2037 V1       EQU   1
                             00000002  00000001  2038 V2       EQU   2
                             00000003  00000001  2039 V3       EQU   3
                             00000004  00000001  2040 V4       EQU   4
                             00000005  00000001  2041 V5       EQU   5
                             00000006  00000001  2042 V6       EQU   6
                             00000007  00000001  2043 V7       EQU   7
                             00000008  00000001  2044 V8       EQU   8
                             00000009  00000001  2045 V9       EQU   9
                             0000000A  00000001  2046 V10      EQU   10
                             0000000B  00000001  2047 V11      EQU   11
                             0000000C  00000001  2048 V12      EQU   12
                             0000000D  00000001  2049 V13      EQU   13
                             0000000E  00000001  2050 V14      EQU   14
                             0000000F  00000001  2051 V15      EQU   15
                             00000010  00000001  2052 V16      EQU   16
                             00000011  00000001  2053 V17      EQU   17
                             00000012  00000001  2054 V18      EQU   18
                             00000013  00000001  2055 V19      EQU   19
                             00000014  00000001  2056 V20      EQU   20
                             00000015  00000001  2057 V21      EQU   21
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2    STMT
                                00000016  00000001  2058 V22      EQU   22
                                00000017  00000001  2059 V23      EQU   23
                                00000018  00000001  2060 V24      EQU   24
                                00000019  00000001  2061 V25      EQU   25
                                0000001A  00000001  2062 V26      EQU   26
                                0000001B  00000001  2063 V27      EQU   27
                                0000001C  00000001  2064 V28      EQU   28
                                0000001D  00000001  2065 V29      EQU   29
                                0000001E  00000001  2066 V30      EQU   30
                                0000001F  00000001  2067 V31      EQU   31
                                                    2068
                                                    2069          END
```

| SYMBOL | TYPE | VALUE | LENGTH | DEFN | REFERENCES |
|---|---|---|---|---|---|
| BEGIN | I | 00000200 | 2 | 157 | 123 153 154 155 |
| CTLR0 | F | 0000048C | 4 | 353 | 167 168 169 170 |
| DECNUM | C | 00001073 | 16 | 404 | 267 269 275 277 |
| E7TEST | 4 | 00000000 | 64 | 418 | 216 |
| E7TESTS | F | 00002A3C | 4 | 1950 | 209 |
| EDIT | X | 00001047 | 18 | 399 | 268 276 |
| ENDTEST | U | 0000031E | 1 | 253 | 214 |
| EOJ | I | 00000470 | 4 | 343 | 202 256 |
| EOJPSW | D | 00000460 | 8 | 341 | 343 |
| FAILCONT | U | 0000030E | 1 | 243 | |
| FAILED | F | 00001000 | 4 | 381 | 245 254 |
| FAILMSG | U | 0000030A | 1 | 237 | 227 |
| FAILPSW | D | 00000478 | 8 | 345 | 347 |
| FAILTEST | I | 00000488 | 4 | 347 | 257 |
| FB0001 | F | 00000280 | 8 | 186 | 190 191 193 |
| IMAGE | 1 | 00000000 | 11032 | 0 | |
| K | U | 00000400 | 1 | 365 | 366 367 368 |
| K64 | U | 00010000 | 1 | 367 | |
| M3 | U | 00000007 | 1 | 422 | 274 |
| MB | U | 00100000 | 1 | 368 | |
| MSG | I | 000003A8 | 4 | 303 | 201 286 |
| MSGCMD | C | 000003F6 | 9 | 333 | 316 317 |
| MSGMSG | C | 000003FF | 95 | 334 | 310 331 308 |
| MSGMVC | I | 000003F0 | 6 | 331 | 314 |
| MSGOK | I | 000003BE | 2 | 312 | 309 |
| MSGRET | I | 000003DE | 4 | 327 | 320 323 |
| MSGSAVE | F | 000003E4 | 4 | 330 | 306 327 |
| NEXTE7 | U | 000002D4 | 1 | 211 | 230 248 |
| OPNAME | C | 00000008 | 8 | 424 | 272 |
| PAGE | U | 00001000 | 1 | 366 | |
| PRT3 | C | 0000105D | 18 | 402 | 268 269 270 276 277 278 |
| PRTLINE | C | 00001008 | 16 | 387 | 394 285 |
| PRTLNG | U | 0000003F | 1 | 394 | 284 |
| PRTM3 | C | 00001044 | 2 | 392 | 278 |
| PRTNAME | C | 00001033 | 8 | 390 | 272 |
| PRTNUM | C | 00001018 | 3 | 388 | 270 |
| R0 | U | 00000000 | 1 | 2015 | 117 167 170 190 192 193 194 199 218 219 244 245 283 284 287 303 306 308 310 312 327 |
| R1 | U | 00000001 | 1 | 2016 | 200 225 226 254 255 285 317 331 545 546 572 573 599 600 626 627 654 655 681 682 708 709 735 736 765 766 792 793 819 820 846 847 876 877 903 904 930 931 957 958 984 985 1020 1021 1047 1048 1074 1075 1101 1102 1129 1130 1156 1157 1183 1184 1210 1211 1240 1241 1267 1268 1294 1295 1321 1322 1351 1352 1378 1379 1405 1406 1432 1433 1459 1460 1495 1496 1522 1523 1549 1550 1576 1577 1604 1605 1631 1632 1658 1659 1685 1686 1715 1716 1742 1743 1769 1770 1796 1797 1826 1827 1853 1854 1880 1881 1907 1908 1934 1935 |
| R10 | U | 0000000A | 1 | 2025 | 155 164 165 |
| R11 | U | 0000000B | 1 | 2026 | 222 223 549 576 603 630 658 685 712 739 769 796 823 850 880 907 934 961 988 1024 1051 1078 1105 1133 1160 1187 1214 1244 1271 1298 1325 1355 1382 1409 1436 1463 1499 1526 1553 1580 1608 1635 1662 1689 1719 1746 1773 1800 1830 1857 1884 1911 1938 |
| R12 | U | 0000000C | 1 | 2027 | 209 212 229 247 |
| R13 | U | 0000000D | 1 | 2028 | |
| R14 | U | 0000000E | 1 | 2029 | |

| SYMBOL | TYPE | VALUE | LENGTH | DEFN | REFERENCES |
|---|---|---|---|---|---|
| R15 | U | 0000000F | 1 | 2030 | 238 263 290 291 |
| R2 | U | 00000002 | 1 | 2017 | 201 266 267 274 275 283 286 287 304 306 312 313 314 316 322 327 328 |
| R3 | U | 00000003 | 1 | 2018 | |
| R4 | U | 00000004 | 1 | 2019 | |
| R5 | U | 00000005 | 1 | 2020 | 212 213 216 264 289 531 551 558 578 585 605 612 632 640 660 667 687 694 714 721 741 751 771 778 798 805 825 832 852 862 882 889 909 916 936 943 963 970 990 1006 1026 1033 1053 1060 1080 1087 1107 1115 1135 1142 1162 1169 1189 1196 1216 1226 1246 1253 1273 1280 1300 1307 1327 1337 1357 1364 1384 1391 1411 1418 1438 1445 1465 1481 1501 1508 1528 1535 1555 1562 1582 1590 1610 1617 1637 1644 1664 1671 1691 1701 1721 1728 1748 1755 1775 1782 1802 1812 1832 1839 1859 1866 1886 1893 1913 1920 1940 |
| R6 | U | 00000006 | 1 | 2021 | |
| R7 | U | 00000007 | 1 | 2022 | |
| R8 | U | 00000008 | 1 | 2023 | 153 157 158 159 161 |
| R9 | U | 00000009 | 1 | 2024 | 154 161 162 164 |
| RE1 | F | 00001114 | 4 | 550 | 537 539 |
| RE10 | F | 00001594 | 4 | 797 | 784 786 |
| RE11 | F | 00001614 | 4 | 824 | 811 813 |
| RE12 | F | 00001694 | 4 | 851 | 838 840 |
| RE13 | F | 00001714 | 4 | 881 | 868 870 |
| RE14 | F | 00001794 | 4 | 908 | 895 897 |
| RE15 | F | 00001814 | 4 | 935 | 922 924 |
| RE16 | F | 00001894 | 4 | 962 | 949 951 |
| RE17 | F | 00001914 | 4 | 989 | 976 978 |
| RE18 | F | 00001994 | 4 | 1025 | 1012 1014 |
| RE19 | F | 00001A14 | 4 | 1052 | 1039 1041 |
| RE2 | F | 00001194 | 4 | 577 | 564 566 |
| RE20 | F | 00001A94 | 4 | 1079 | 1066 1068 |
| RE21 | F | 00001B14 | 4 | 1106 | 1093 1095 |
| RE22 | F | 00001B94 | 4 | 1134 | 1121 1123 |
| RE23 | F | 00001C14 | 4 | 1161 | 1148 1150 |
| RE24 | F | 00001C94 | 4 | 1188 | 1175 1177 |
| RE25 | F | 00001D14 | 4 | 1215 | 1202 1204 |
| RE26 | F | 00001D94 | 4 | 1245 | 1232 1234 |
| RE27 | F | 00001E14 | 4 | 1272 | 1259 1261 |
| RE28 | F | 00001E94 | 4 | 1299 | 1286 1288 |
| RE29 | F | 00001F14 | 4 | 1326 | 1313 1315 |
| RE3 | F | 00001214 | 4 | 604 | 591 593 |
| RE30 | F | 00001F94 | 4 | 1356 | 1343 1345 |
| RE31 | F | 00002014 | 4 | 1383 | 1370 1372 |
| RE32 | F | 00002094 | 4 | 1410 | 1397 1399 |
| RE33 | F | 00002114 | 4 | 1437 | 1424 1426 |
| RE34 | F | 00002194 | 4 | 1464 | 1451 1453 |
| RE35 | F | 00002214 | 4 | 1500 | 1487 1489 |
| RE36 | F | 00002294 | 4 | 1527 | 1514 1516 |
| RE37 | F | 00002314 | 4 | 1554 | 1541 1543 |
| RE38 | F | 00002394 | 4 | 1581 | 1568 1570 |
| RE39 | F | 00002414 | 4 | 1609 | 1596 1598 |
| RE4 | F | 00001294 | 4 | 631 | 618 620 |
| RE40 | F | 00002494 | 4 | 1636 | 1623 1625 |
| RE41 | F | 00002514 | 4 | 1663 | 1650 1652 |
| RE42 | F | 00002594 | 4 | 1690 | 1677 1679 |
| RE43 | F | 00002614 | 4 | 1720 | 1707 1709 |

| SYMBOL | TYPE | VALUE | LENGTH | DEFN | REFERENCES |
|---|---|---|---|---|---|
| RE44 | F | 00002694 | 4 | 1747 | 1734 1736 |
| RE45 | F | 00002714 | 4 | 1774 | 1761 1763 |
| RE46 | F | 00002794 | 4 | 1801 | 1788 1790 |
| RE47 | F | 00002814 | 4 | 1831 | 1818 1820 |
| RE48 | F | 00002894 | 4 | 1858 | 1845 1847 |
| RE49 | F | 00002914 | 4 | 1885 | 1872 1874 |
| RE5 | F | 00001314 | 4 | 659 | 646 648 |
| RE50 | F | 00002994 | 4 | 1912 | 1899 1901 |
| RE51 | F | 00002A14 | 4 | 1939 | 1926 1928 |
| RE6 | F | 00001394 | 4 | 686 | 673 675 |
| RE7 | F | 00001414 | 4 | 713 | 700 702 |
| RE8 | F | 00001494 | 4 | 740 | 727 729 |
| RE9 | F | 00001514 | 4 | 770 | 757 759 |
| REA1 | A | 000010D0 | 4 | 539 | |
| REA10 | A | 00001550 | 4 | 786 | |
| REA11 | A | 000015D0 | 4 | 813 | |
| REA12 | A | 00001650 | 4 | 840 | |
| REA13 | A | 000016D0 | 4 | 870 | |
| REA14 | A | 00001750 | 4 | 897 | |
| REA15 | A | 000017D0 | 4 | 924 | |
| REA16 | A | 00001850 | 4 | 951 | |
| REA17 | A | 000018D0 | 4 | 978 | |
| REA18 | A | 00001950 | 4 | 1014 | |
| REA19 | A | 000019D0 | 4 | 1041 | |
| REA2 | A | 00001150 | 4 | 566 | |
| REA20 | A | 00001A50 | 4 | 1068 | |
| REA21 | A | 00001AD0 | 4 | 1095 | |
| REA22 | A | 00001B50 | 4 | 1123 | |
| REA23 | A | 00001BD0 | 4 | 1150 | |
| REA24 | A | 00001C50 | 4 | 1177 | |
| REA25 | A | 00001CD0 | 4 | 1204 | |
| REA26 | A | 00001D50 | 4 | 1234 | |
| REA27 | A | 00001DD0 | 4 | 1261 | |
| REA28 | A | 00001E50 | 4 | 1288 | |
| REA29 | A | 00001ED0 | 4 | 1315 | |
| REA3 | A | 000011D0 | 4 | 593 | |
| REA30 | A | 00001F50 | 4 | 1345 | |
| REA31 | A | 00001FD0 | 4 | 1372 | |
| REA32 | A | 00002050 | 4 | 1399 | |
| REA33 | A | 000020D0 | 4 | 1426 | |
| REA34 | A | 00002150 | 4 | 1453 | |
| REA35 | A | 000021D0 | 4 | 1489 | |
| REA36 | A | 00002250 | 4 | 1516 | |
| REA37 | A | 000022D0 | 4 | 1543 | |
| REA38 | A | 00002350 | 4 | 1570 | |
| REA39 | A | 000023D0 | 4 | 1598 | |
| REA4 | A | 00001250 | 4 | 620 | |
| REA40 | A | 00002450 | 4 | 1625 | |
| REA41 | A | 000024D0 | 4 | 1652 | |
| REA42 | A | 00002550 | 4 | 1679 | |
| REA43 | A | 000025D0 | 4 | 1709 | |
| REA44 | A | 00002650 | 4 | 1736 | |
| REA45 | A | 000026D0 | 4 | 1763 | |
| REA46 | A | 00002750 | 4 | 1790 | |
| REA47 | A | 000027D0 | 4 | 1820 | |
| REA48 | A | 00002850 | 4 | 1847 | |

| SYMBOL | TYPE | VALUE | LENGTH | DEFN | REFERENCES | | |
|---|---|---|---|---|---|---|---|
| REA49 | A | 000028D0 | 4 | 1874 | | | |
| REA5 | A | 000012D0 | 4 | 648 | | | |
| REA50 | A | 00002950 | 4 | 1901 | | | |
| REA51 | A | 000029D0 | 4 | 1928 | | | |
| REA6 | A | 00001350 | 4 | 675 | | | |
| REA7 | A | 000013D0 | 4 | 702 | | | |
| REA8 | A | 00001450 | 4 | 729 | | | |
| REA9 | A | 000014D0 | 4 | 759 | | | |
| READDR | A | 00000018 | 4 | 427 | 225 | | |
| REG2LOW | U | 000000DD | 1 | 371 | | | |
| REG2PATT | U | AABBCCDD | 1 | 370 | | | |
| RELEN | A | 00000014 | 4 | 426 | | | |
| RPTDWSAV | D | 00000398 | 8 | 296 | 283 | 287 | |
| RPTERROR | I | 0000032C | 4 | 263 | 238 | | |
| RPTSAVE | F | 00000390 | 4 | 293 | 263 | 290 | |
| RPTSVR5 | F | 00000394 | 4 | 294 | 264 | 289 | |
| SKL0001 | U | 0000004E | 1 | 183 | 199 | | |
| SKT0001 | C | 0000022A | 20 | 180 | 183 | 200 | |
| SVOLDPSW | U | 00000140 | 0 | 119 | | | |
| T1 | A | 000010B8 | 4 | 532 | 1953 | | |
| T10 | A | 00001538 | 4 | 779 | 1962 | | |
| T11 | A | 000015B8 | 4 | 806 | 1963 | | |
| T12 | A | 00001638 | 4 | 833 | 1964 | | |
| T13 | A | 000016B8 | 4 | 863 | 1965 | | |
| T14 | A | 00001738 | 4 | 890 | 1966 | | |
| T15 | A | 000017B8 | 4 | 917 | 1967 | | |
| T16 | A | 00001838 | 4 | 944 | 1968 | | |
| T17 | A | 000018B8 | 4 | 971 | 1969 | | |
| T18 | A | 00001938 | 4 | 1007 | 1970 | | |
| T19 | A | 000019B8 | 4 | 1034 | 1971 | | |
| T2 | A | 00001138 | 4 | 559 | 1954 | | |
| T20 | A | 00001A38 | 4 | 1061 | 1972 | | |
| T21 | A | 00001AB8 | 4 | 1088 | 1973 | | |
| T22 | A | 00001B38 | 4 | 1116 | 1974 | | |
| T23 | A | 00001BB8 | 4 | 1143 | 1975 | | |
| T24 | A | 00001C38 | 4 | 1170 | 1976 | | |
| T25 | A | 00001CB8 | 4 | 1197 | 1977 | | |
| T26 | A | 00001D38 | 4 | 1227 | 1978 | | |
| T27 | A | 00001DB8 | 4 | 1254 | 1979 | | |
| T28 | A | 00001E38 | 4 | 1281 | 1980 | | |
| T29 | A | 00001EB8 | 4 | 1308 | 1981 | | |
| T3 | A | 000011B8 | 4 | 586 | 1955 | | |
| T30 | A | 00001F38 | 4 | 1338 | 1982 | | |
| T31 | A | 00001FB8 | 4 | 1365 | 1983 | | |
| T32 | A | 00002038 | 4 | 1392 | 1984 | | |
| T33 | A | 000020B8 | 4 | 1419 | 1985 | | |
| T34 | A | 00002138 | 4 | 1446 | 1986 | | |
| T35 | A | 000021B8 | 4 | 1482 | 1987 | | |
| T36 | A | 00002238 | 4 | 1509 | 1988 | | |
| T37 | A | 000022B8 | 4 | 1536 | 1989 | | |
| T38 | A | 00002338 | 4 | 1563 | 1990 | | |
| T39 | A | 000023B8 | 4 | 1591 | 1991 | | |
| T4 | A | 00001238 | 4 | 613 | 1956 | | |
| T40 | A | 00002438 | 4 | 1618 | 1992 | | |
| T41 | A | 000024B8 | 4 | 1645 | 1993 | | |
| T42 | A | 00002538 | 4 | 1672 | 1994 | | |

| SYMBOL | TYPE | VALUE | LENGTH | DEFN | REFERENCES |
|---|---|---|---|---|---|
| T43 | A | 000025B8 | 4 | 1702 | 1995 |
| T44 | A | 00002638 | 4 | 1729 | 1996 |
| T45 | A | 000026B8 | 4 | 1756 | 1997 |
| T46 | A | 00002738 | 4 | 1783 | 1998 |
| T47 | A | 000027B8 | 4 | 1813 | 1999 |
| T48 | A | 00002838 | 4 | 1840 | 2000 |
| T49 | A | 000028B8 | 4 | 1867 | 2001 |
| T5 | A | 000012B8 | 4 | 641 | 1957 |
| T50 | A | 00002938 | 4 | 1894 | 2002 |
| T51 | A | 000029B8 | 4 | 1921 | 2003 |
| T6 | A | 00001338 | 4 | 668 | 1958 |
| T7 | A | 000013B8 | 4 | 695 | 1959 |
| T8 | A | 00001438 | 4 | 722 | 1960 |
| T9 | A | 000014B8 | 4 | 752 | 1961 |
| TESTING | F | 00001004 | 4 | 382 | 219 |
| TNUM | H | 00000004 | 2 | 420 | 218 266 |
| TSUB | A | 00000000 | 4 | 419 | 222 |
| TTABLE | F | 00002A3C | 4 | 1952 | |
| V0 | U | 00000000 | 1 | 2036 | |
| V1 | U | 00000001 | 1 | 2037 | 221 |
| V10 | U | 0000000A | 1 | 2046 | |
| V11 | U | 0000000B | 1 | 2047 | |
| V12 | U | 0000000C | 1 | 2048 | |
| V13 | U | 0000000D | 1 | 2049 | |
| V14 | U | 0000000E | 1 | 2050 | |
| V15 | U | 0000000F | 1 | 2051 | |
| V16 | U | 00000010 | 1 | 2052 | |
| V17 | U | 00000011 | 1 | 2053 | |
| V18 | U | 00000012 | 1 | 2054 | |
| V19 | U | 00000013 | 1 | 2055 | |
| V1FUDGE | X | 00001094 | 16 | 411 | 221 |
| V1O1 | X | 000010E0 | 16 | 541 | 548 |
| V1O10 | X | 00001560 | 16 | 788 | 795 |
| V1O11 | X | 000015E0 | 16 | 815 | 822 |
| V1O12 | X | 00001660 | 16 | 842 | 849 |
| V1O13 | X | 000016E0 | 16 | 872 | 879 |
| V1O14 | X | 00001760 | 16 | 899 | 906 |
| V1O15 | X | 000017E0 | 16 | 926 | 933 |
| V1O16 | X | 00001860 | 16 | 953 | 960 |
| V1O17 | X | 000018E0 | 16 | 980 | 987 |
| V1O18 | X | 00001960 | 16 | 1016 | 1023 |
| V1O19 | X | 000019E0 | 16 | 1043 | 1050 |
| V1O2 | X | 00001160 | 16 | 568 | 575 |
| V1O20 | X | 00001A60 | 16 | 1070 | 1077 |
| V1O21 | X | 00001AE0 | 16 | 1097 | 1104 |
| V1O22 | X | 00001B60 | 16 | 1125 | 1132 |
| V1O23 | X | 00001BE0 | 16 | 1152 | 1159 |
| V1O24 | X | 00001C60 | 16 | 1179 | 1186 |
| V1O25 | X | 00001CE0 | 16 | 1206 | 1213 |
| V1O26 | X | 00001D60 | 16 | 1236 | 1243 |
| V1O27 | X | 00001DE0 | 16 | 1263 | 1270 |
| V1O28 | X | 00001E60 | 16 | 1290 | 1297 |
| V1O29 | X | 00001EE0 | 16 | 1317 | 1324 |
| V1O3 | X | 000011E0 | 16 | 595 | 602 |
| V1O30 | X | 00001F60 | 16 | 1347 | 1354 |
| V1O31 | X | 00001FE0 | 16 | 1374 | 1381 |

| SYMBOL | TYPE | VALUE | LENGTH | DEFN | REFERENCES |
|---|---|---|---|---|---|
| V1032 | X | 00002060 | 16 | 1401 | 1408 |
| V1033 | X | 000020E0 | 16 | 1428 | 1435 |
| V1034 | X | 00002160 | 16 | 1455 | 1462 |
| V1035 | X | 000021E0 | 16 | 1491 | 1498 |
| V1036 | X | 00002260 | 16 | 1518 | 1525 |
| V1037 | X | 000022E0 | 16 | 1545 | 1552 |
| V1038 | X | 00002360 | 16 | 1572 | 1579 |
| V1039 | X | 000023E0 | 16 | 1600 | 1607 |
| V104 | X | 00001260 | 16 | 622 | 629 |
| V1040 | X | 00002460 | 16 | 1627 | 1634 |
| V1041 | X | 000024E0 | 16 | 1654 | 1661 |
| V1042 | X | 00002560 | 16 | 1681 | 1688 |
| V1043 | X | 000025E0 | 16 | 1711 | 1718 |
| V1044 | X | 00002660 | 16 | 1738 | 1745 |
| V1045 | X | 000026E0 | 16 | 1765 | 1772 |
| V1046 | X | 00002760 | 16 | 1792 | 1799 |
| V1047 | X | 000027E0 | 16 | 1822 | 1829 |
| V1048 | X | 00002860 | 16 | 1849 | 1856 |
| V1049 | X | 000028E0 | 16 | 1876 | 1883 |
| V105 | X | 000012E0 | 16 | 650 | 657 |
| V1050 | X | 00002960 | 16 | 1903 | 1910 |
| V1051 | X | 000029E0 | 16 | 1930 | 1937 |
| V106 | X | 00001360 | 16 | 677 | 684 |
| V107 | X | 000013E0 | 16 | 704 | 711 |
| V108 | X | 00001460 | 16 | 731 | 738 |
| V109 | X | 000014E0 | 16 | 761 | 768 |
| V1OUTPUT | X | 00000028 | 16 | 429 | 226 |
| V2 | U | 00000002 | 1 | 2038 | |
| V20 | U | 00000014 | 1 | 2056 | |
| V21 | U | 00000015 | 1 | 2057 | |
| V22 | U | 00000016 | 1 | 2058 | 546 547 548 573 574 575 600 601 602 627 628 629 655 656 657 682 683 684 709 710 711 736 737 738 766 767 768 793 794 795 820 821 822 847 848 849 877 878 879 904 905 906 931 932 933 958 959 960 985 986 987 1021 1022 1023 1048 1049 1050 1075 1076 1077 1102 1103 1104 1130 1131 1132 1157 1158 1159 1184 1185 1186 1211 1212 1213 1241 1242 1243 1268 1269 1270 1295 1296 1297 1322 1323 1324 1352 1353 1354 1379 1380 1381 1406 1407 1408 1433 1434 1435 1460 1461 1462 1496 1497 1498 1523 1524 1525 1550 1551 1552 1577 1578 1579 1605 1606 1607 1632 1633 1634 1659 1660 1661 1686 1687 1688 1716 1717 1718 1743 1744 1745 1770 1771 1772 1797 1798 1799 1827 1828 1829 1854 1855 1856 1881 1882 1883 1908 1909 1910 1935 1936 1937 |
| V23 | U | 00000017 | 1 | 2059 | |
| V24 | U | 00000018 | 1 | 2060 | |
| V25 | U | 00000019 | 1 | 2061 | |
| V26 | U | 0000001A | 1 | 2062 | |
| V27 | U | 0000001B | 1 | 2063 | |
| V28 | U | 0000001C | 1 | 2064 | |
| V29 | U | 0000001D | 1 | 2065 | |
| V2ADDR | A | 00000010 | 4 | 425 | 545 572 599 626 654 681 708 735 765 792 819 846 876 903 930 957 984 1020 1047 1074 1101 1129 1156 1183 1210 1240 1267 1294 1321 1351 1378 1405 1432 1459 1495 1522 1549 1576 1604 1631 1658 1685 1715 1742 1769 1796 1826 1853 1880 1907 1934 |
| V3 | U | 00000003 | 1 | 2039 | |
| V30 | U | 0000001E | 1 | 2066 | |
| V31 | U | 0000001F | 1 | 2067 | |

| SYMBOL | TYPE | VALUE | LENGTH | DEFN | REFERENCES |
|---|---|---|---|---|---|
| V4 | U | 00000004 | 1 | 2040 | |
| V5 | U | 00000005 | 1 | 2041 | |
| V6 | U | 00000006 | 1 | 2042 | |
| V7 | U | 00000007 | 1 | 2043 | |
| V8 | U | 00000008 | 1 | 2044 | |
| V9 | U | 00000009 | 1 | 2045 | |
| X0001 | U | 000002A8 | 1 | 189 | 177 190 |
| X1 | F | 000010F8 | 4 | 544 | 532 |
| X10 | F | 00001578 | 4 | 791 | 779 |
| X11 | F | 000015F8 | 4 | 818 | 806 |
| X12 | F | 00001678 | 4 | 845 | 833 |
| X13 | F | 000016F8 | 4 | 875 | 863 |
| X14 | F | 00001778 | 4 | 902 | 890 |
| X15 | F | 000017F8 | 4 | 929 | 917 |
| X16 | F | 00001878 | 4 | 956 | 944 |
| X17 | F | 000018F8 | 4 | 983 | 971 |
| X18 | F | 00001978 | 4 | 1019 | 1007 |
| X19 | F | 000019F8 | 4 | 1046 | 1034 |
| X2 | F | 00001178 | 4 | 571 | 559 |
| X20 | F | 00001A78 | 4 | 1073 | 1061 |
| X21 | F | 00001AF8 | 4 | 1100 | 1088 |
| X22 | F | 00001B78 | 4 | 1128 | 1116 |
| X23 | F | 00001BF8 | 4 | 1155 | 1143 |
| X24 | F | 00001C78 | 4 | 1182 | 1170 |
| X25 | F | 00001CF8 | 4 | 1209 | 1197 |
| X26 | F | 00001D78 | 4 | 1239 | 1227 |
| X27 | F | 00001DF8 | 4 | 1266 | 1254 |
| X28 | F | 00001E78 | 4 | 1293 | 1281 |
| X29 | F | 00001EF8 | 4 | 1320 | 1308 |
| X3 | F | 000011F8 | 4 | 598 | 586 |
| X30 | F | 00001F78 | 4 | 1350 | 1338 |
| X31 | F | 00001FF8 | 4 | 1377 | 1365 |
| X32 | F | 00002078 | 4 | 1404 | 1392 |
| X33 | F | 000020F8 | 4 | 1431 | 1419 |
| X34 | F | 00002178 | 4 | 1458 | 1446 |
| X35 | F | 000021F8 | 4 | 1494 | 1482 |
| X36 | F | 00002278 | 4 | 1521 | 1509 |
| X37 | F | 000022F8 | 4 | 1548 | 1536 |
| X38 | F | 00002378 | 4 | 1575 | 1563 |
| X39 | F | 000023F8 | 4 | 1603 | 1591 |
| X4 | F | 00001278 | 4 | 625 | 613 |
| X40 | F | 00002478 | 4 | 1630 | 1618 |
| X41 | F | 000024F8 | 4 | 1657 | 1645 |
| X42 | F | 00002578 | 4 | 1684 | 1672 |
| X43 | F | 000025F8 | 4 | 1714 | 1702 |
| X44 | F | 00002678 | 4 | 1741 | 1729 |
| X45 | F | 000026F8 | 4 | 1768 | 1756 |
| X46 | F | 00002778 | 4 | 1795 | 1783 |
| X47 | F | 000027F8 | 4 | 1825 | 1813 |
| X48 | F | 00002878 | 4 | 1852 | 1840 |
| X49 | F | 000028F8 | 4 | 1879 | 1867 |
| X5 | F | 000012F8 | 4 | 653 | 641 |
| X50 | F | 00002978 | 4 | 1906 | 1894 |
| X51 | F | 000029F8 | 4 | 1933 | 1921 |
| X6 | F | 00001378 | 4 | 680 | 668 |
| X7 | F | 000013F8 | 4 | 707 | 695 |

| SYMBOL | TYPE | VALUE | LENGTH | DEFN | REFERENCES |
|---|---|---|---|---|---|
| X8 | F | 00001478 | 4 | 734 | 722 |
| X9 | F | 000014F8 | 4 | 764 | 752 |
| XC0001 | U | 000002D0 | 1 | 203 | 195 |
| ZVE7TST | J | 00000000 | 11032 | 116 | 119 121 125 129 380 117 |
| =A(E7TESTS) | A | 00000498 | 4 | 358 | 209 |
| =AL2(L'MSGMSG) | R | 000004A2 | 2 | 361 | 308 |
| =F'1' | F | 0000049C | 4 | 359 | 244 |
| =F'64' | F | 00000494 | 4 | 357 | 194 |
| =H'0' | H | 000004A0 | 2 | 360 | 303 |

```
 MACRO    DEFN   REFERENCES

FCHECK     69    176
PTTABLE   489   1951
VRR_A     448    529    556    583    610    638    665    692    719    749    776    803    830    860    887    914    941    968
                1004   1031   1058   1085   1113   1140   1167   1194   1224   1251   1278   1305   1335   1362   1389   1416   1443
                1479   1506   1533   1560   1588   1615   1642   1669   1699   1726   1753   1780   1810   1837   1864   1891   1918
```

```
   DESC      SYMBOL    SIZE      POS         ADDR

Entry: 0

Image       IMAGE     11032   0000-2B17   0000-2B17
  Region              11032   0000-2B17   0000-2B17
    CSECT   ZVE7TST   11032   0000-2B17   0000-2B17
```

```
   STMT                          FILE NAME
1     /home/tn529/sharedvfp/tests/zvector-e7-04-BitCount.asm

** NO ERRORS FOUND **
```