```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    2 ************************************************************************
                                                    3 *
                                                    4 *        EXPERIMENTAL pending further PoP definition
                                                    5 *
                                                    6 *        Zvector E6 instruction tests for VRR-a encoded:
                                                    7 *
                                                    8 *        E655 VCNF     - VECTOR FP CONVERT TO NNP
                                                    9 *        E656 VCLFNH   - VECTOR FP CONVERT AND LENGTHEN FROM NNP HIGH
                                                   10 *        E65D VCFN     - VECTOR FP CONVERT FROM NNP
                                                   11 *        E65E VCLFNL   - VECTOR FP CONVERT AND LENGTHEN FROM NNP LOW
                                                   12 *
                                                   13 *        and partial testing of
                                                   14 *
                                                   15 *        E675  VCRNF   - VECTOR FP CONVERT AND ROUND TO NNP
                                                   16 *
                                                   17 *        during cross check tests for VCLFNH and VCLFNL
                                                   18 *
                                                   19 *        James Wekel August 2024
                                                   20 ************************************************************************

                                                   22 ************************************************************************
                                                   23 *
                                                   24 *        basic instruction tests
                                                   25 *
                                                   26 ************************************************************************
                                                   27 *  This program tests EXPERIMENTAL functioning of the z/arch E6 VRR-a
                                                   28 *  Neural-network-processing-assist facility vector instructions.
                                                   29 *  These test are EXPERIMENTAL pending further PoP definition of
                                                   30 *  NNP-data-type-1.
                                                   31 *
                                                   32 *  If requested and if VXC == 0 after test instruction execution,
                                                   33 *  a cross check test is performed. A cross check uses the result
                                                   34 *  of the instruction test to recreate the test source.
                                                   35 *
                                                   36 *  Exceptions (including trapable IEEE exceptions) are not tested.
                                                   37 *
                                                   38 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                   39 *  obvious coding errors.  None of the tests are thorough.  They are
                                                   40 *  NOT designed to test all aspects of any of the instructions.
                                                   41 *
                                                   42 ************************************************************************
                                                   43 *
                                                   44 *    *Testcase zvector-e6-20-NNPconvert
                                                   45 *    *
                                                   46 *    *   EXPERIMENTAL pending further PoP definition
                                                   47 *    *
                                                   48 *    *   Zvector E6 instruction tests for VRR-a encoded:
                                                   49 *    *
                                                   50 *    *   E655 VCNF     - VECTOR FP CONVERT TO NNP
                                                   51 *    *   E656 VCLFNH   - VECTOR FP CONVERT AND LENGTHEN FROM NNP HIGH
                                                   52 *    *   E65D VCFN     - VECTOR FP CONVERT FROM NNP
                                                   53 *    *   E65E VCLFNL   - VECTOR FP CONVERT AND LENGTHEN FROM NNP LOW
                                                   54 *    *
                                                   55 *    *   # ---------------------------------------------------------
                                                   56 *    *   #  This tests only the basic function of the instruction.
```

```
 LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                     57 *    *   #  Exceptions are NOT tested.
                                                     58 *    *   # ------------------------------------------------------
                                                     59 *    *
                                                     60 *    mainsize    2
                                                     61 *    numcpu      1
                                                     62 *    sysclear
                                                     63 *    archlvl     z/Arch
                                                     64 *
                                                     65 *    loadcore    "$(testpath)/zvector-e6-20-NNPconvert.core" 0x0
                                                     66 *
                                                     67 *    diag8cmd    enable    # (needed for messages to Hercules console)
                                                     68 *    runtest 2
                                                     69 *    diag8cmd    disable   # (reset back to default)
                                                     70 *
                                                     71 *    *Done
                                                     72 *
                                                     73 ********************************************************************************
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                       75 ************************************************************************
                                                       76 *        FCHECK Macro - Is a Facility Bit set?
                                                       77 *
                                                       78 *        If the facility bit is NOT set, an message is issued and
                                                       79 *        the test is skipped.
                                                       80 *
                                                       81 *        Fcheck uses R0, R1 and R2
                                                       82 *
                                                       83 * eg.    FCHECK 134,'vector-packed-decimal'
                                                       84 ************************************************************************
                                                       85          MACRO
                                                       86          FCHECK &BITNO,&NOTSETMSG
                                                       87 .*                      &BITNO : facility bit number to check
                                                       88 .*                      &NOTSETMSG : 'facility name'
                                                       89          LCLA  &FBBYTE           Facility bit in Byte
                                                       90          LCLA  &FBBIT            Facility bit within Byte
                                                       91
                                                       92          LCLA  &L(8)
                                                       93 &L(1)    SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                                       94
                                                       95 &FBBYTE  SETA  &BITNO/8
                                                       96 &FBBIT   SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                                       97 .*       MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                                       98
                                                       99          B     X&SYSNDX
                                                      100 *                                     Fcheck data area
                                                      101 *                                     skip messgae
                                                      102 SKT&SYSNDX DC  C'          Skipping tests: '
                                                      103          DC    C&NOTSETMSG
                                                      104          DC    C' facility (bit &BITNO) is not installed.'
                                                      105 SKL&SYSNDX EQU *-SKT&SYSNDX
                                                      106 *                                     facility bits
                                                      107          DS    FD                     gap
                                                      108 FB&SYSNDX DS   4FD
                                                      109          DS    FD                     gap
                                                      110 *
                                                      111 X&SYSNDX EQU *
                                                      112          LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                                      113          STFLE FB&SYSNDX              get facility bits
                                                      114
                                                      115          XGR   R0,R0
                                                      116          IC    R0,FB&SYSNDX+&FBBYTE   get fbit byte
                                                      117          N     R0,=F'&FBBIT'          is bit set?
                                                      118          BNZ   XC&SYSNDX
                                                      119 *
                                                      120 * facility bit not set, issue message and exit
                                                      121 *
                                                      122          LA    R0,SKL&SYSNDX          message length
                                                      123          LA    R1,SKT&SYSNDX          message address
                                                      124          BAL   R2,MSG
                                                      125
                                                      126          B     EOJ
                                                      127 XC&SYSNDX EQU *
                                                      128          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     130 ********************************************************************************
                                                     131 *        Low core PSWs
                                                     132 ********************************************************************************


                             00000000  00003997    134 ZVE6TST  START 0
00000000                     00000000                135          USING ZVE6TST,R0            Low core addressability
                                                     136
                             00000140  00000000    137 SVOLDPSW EQU   ZVE6TST+X'140'        z/Arch Supervisor call old PSW


00000000                     00000000  000001A0    139          ORG   ZVE6TST+X'1A0'        z/Architecure RESTART PSW
000001A0  00000001 80000000                      140          DC    X'0000000180000000'
000001A8  00000000 00000200                      141          DC    AD(BEGIN)


000001B0                     000001B0  000001D0    143          ORG   ZVE6TST+X'1D0'        z/Architecure PROGRAM CHECK PSW
000001D0  00020001 80000000                      144          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                      145          DC    AD(X'DEAD')


000001E0                     000001E0  00000200    147          ORG   ZVE6TST+X'200'        Start of actual test program...
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                     149
                                                     150 ********************************************************************************
                                                     151 *                The actual "ZVE6TST" program itself...
                                                     152 ********************************************************************************
                                                     153 *
                                                     154 *  Architecture Mode: z/Arch
                                                     155 *  Register Usage:
                                                     156 *
                                                     157 *   R0       (work)
                                                     158 *   R1-4     (work)
                                                     159 *   R5       Testing control table - current test base
                                                     160 *   R6-R7    (work)
                                                     161 *   R8       First base register
                                                     162 *   R9       Second base register
                                                     163 *   R10      Third base register
                                                     164 *   R11      E6TEST call return
                                                     165 *   R12      E6TESTS register
                                                     166 *   R13      (work)
                                                     167 *   R14      Subroutine call
                                                     168 *   R15      Secondary Subroutine call or work
                                                     169 *
                                                     170 ********************************************************************************

00000200                        00000200             172          USING  BEGIN,R8                FIRST Base Register
00000200                        00001200             173          USING  BEGIN+4096,R9           SECOND Base Register
00000200                        00002200             174          USING  BEGIN+8192,R10          THIRD Base Register
                                                     175
00000200  0580                                       176 BEGIN    BALR   R8,0                    Initalize FIRST base register
00000202  0680                                       177          BCTR   R8,0                    Initalize FIRST base register
00000204  0680                                       178          BCTR   R8,0                    Initalize FIRST base register
                                                     179
00000206  4190 8800                      00000800    180          LA     R9,2048(,R8)            Initalize SECOND base register
0000020A  4190 9800                      00000800    181          LA     R9,2048(,R9)            Initalize SECOND base register
                                                     182
0000020E  41A0 9800                      00000800    183          LA     R10,2048(,R9)           Initalize THIRD base register
00000212  41A0 A800                      00000800    184          LA     R10,2048(,R10)          Initalize THIRD base register
                                                     185
00000216  B600 84BC                      000006BC    186          STCTL  R0,R0,CTLR0             Store CR0 to enable AFP
0000021A  9604 84BD                      000006BD    187          OI     CTLR0+1,X'04'           Turn on AFP bit
0000021E  9602 84BD                      000006BD    188          OI     CTLR0+1,X'02'           Turn on Vector bit
00000222  B700 84BC                      000006BC    189          LCTL   R0,R0,CTLR0             Reload updated CR0
                                                     190
                                                     191 ********************************************************************************
                                                     192 * Is Neural-network-processing-assist facility 2 installed  (bit 165)
                                                     193 ********************************************************************************
                                                     194
                                                     195          FCHECK 165,'Neural-network-processing-assist'
00000226  47F0 80C0                      000002C0    196+         B      X0001
                                                     197+*                                       Fcheck data area
                                                     198+*                                       skip messgae
0000022A  40404040 40404040                          199+SKT0001  DC     C'          Skipping tests: '
00000244  D585A499 81936095                          200+         DC     C'Neural-network-processing-assist'
00000264  40868183 899389A3                          201+         DC     C' facility (bit 165) is not installed.'
                            0000005F  00000001       202+SKL0001  EQU    *-SKT0001
                                                     203+*                                       facility bits
00000290  00000000 00000000                          204+         DS     FD                      gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00000298  00000000 00000000                        205+FB0001   DS    4FD
000002B8  00000000 00000000                        206+         DS    FD                        gap
                                                   207+*
                             000002C0  00000001    208+X0001    EQU   *
000002C0  4100 0004                    00000004    209+         LA    R0,((X0001-FB0001)/8)-1
000002C4  B2B0 8098                    00000298    210+         STFLE FB0001                    get facility bits
000002C8  B982 0000                                211+         XGR   R0,R0
000002CC  4300 80AC                    000002AC    212+         IC    R0,FB0001+20              get fbit byte
000002D0  5400 84F8                    000006F8    213+         N     R0,=F'4'                  is bit set?
000002D4  4770 80E8                    000002E8    214+         BNZ   XC0001
                                                   215+*
                                                   216+* facility bit not set, issue message and exit
                                                   217+*
000002D8  4100 005F                    0000005F    218+         LA    R0,SKL0001                message length
000002DC  4110 802A                    0000022A    219+         LA    R1,SKT0001                message address
000002E0  4520 83D8                    000005D8    220+         BAL   R2,MSG
000002E4  47F0 84A0                    000006A0    221+         B     EOJ
                             000002E8  00000001    222+XC0001   EQU   *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     224 ********************************************************************************
                                                     225 *               Do tests in the E6TESTS table
                                                     226 ********************************************************************************
                                                     227
000002E8  58C0 84FC                       000006FC  228           L     R12,=A(E6TESTS)         get table of test addresses
                                                     229
                               000002EC  00000001  230 NEXTE6    EQU   *
000002EC  5850 C000                       00000000  231           L     R5,0(0,R12)             get test address
000002F0  1255                                      232           LTR   R5,R5                      have a test?
000002F2  4780 8390                       00000590  233           BZ    ENDTEST                       done?
                                                     234
000002F6                       00000000             235           USING E6TEST,R5
                                                     236
000002F6  4800 5004                       00000004  237           LH    R0,TNUM                 save current test number
000002FA  5000 8E04                       00001004  238           ST    R0,TESTING              for easy reference
                                                     239
000002FE  58B0 5000                       00000000  240           L     R11,TSUB                get address of test routine
00000302  05BB                                      241           BALR  R11,R11                 do test
                                                     242
00000304  45F0 8146                       00000346  243           BAL   R15,XCHECK
                                                     244 *
                                                     245 * validate FPC first
                                                     246 *
00000308  D500 500A 5041                  00000041  247           CLC   FLG(1),FPC_R+1          expected FPC flags?
0000030E  4770 8318                       00000518  248           BNE   FAILMSG                 no, issue failed message
00000312  D500 500B 5042                  00000042  249           CLC   VXC(1),FPC_R+2          expected VXC?
00000318  4770 8318                       00000518  250           BNE   FAILMSG                 no, issue failed message
                                                     251
                                                     252 * then validate results, if not inexact
                                                     253
0000031C  B982 0011                                 254           XGR   R1,R1
00000320  4310 5041                       00000041  255           IC    R1,FPC_R+1              FPC flags
00000324  5410 8500                       00000700  256           N     R1,=XL4'00000008'       check inexact flag
00000328  1211                                      257           LTR   R1,R1
0000032A  4770 813E                       0000033E  258           BNZ   DONEXT
                                                     259
0000032E  E310 501C 0014                  0000001C  260           LGF   R1,READDR               expected result address
00000334  D50F 5028 1000       00000028  00000000  261           CLC   V1OUTPUT,0(R1)
0000033A  4770 8318                       00000518  262           BNE   FAILMSG                 no, issue failed message
                                                     263
                               0000033E  00000001  264 DONEXT    EQU   *
0000033E  41C0 C004                       00000004  265           LA    R12,4(0,R12)            next test address
00000342  47F0 80EC                       000002EC  266           B     NEXTE6
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    268 *-------------------------------------------------------------------
                                                    269 * cross check that the result can be converted back to the source
                                                    270 * where there were NO exceptions (DXC/VXC = 0)
                                                    271 *-------------------------------------------------------------------
                                 00000346  00000001 272 XCHECK   EQU   *
00000346  D207 5050 84C8         00000050  000006C8 273           MVC   SKIPXC,=CL8'SKIP XC '
0000034C  D500 5007 850C         00000007  0000070C 274           CLC   XCSKIP,=CL1'S'          skip xcheck requested
00000352  478F 0000                        00000000 275           BE    0(R15)                  skip = S, so exit
00000356  9500 5042                        00000042 276           CLI   FPC_R+2,0               Only Xcheck no VXC error
0000035A  477F 0000                        00000000 277           BNZ   0(R15)                  some VXC error , so exit
                                                    278 *
                                                    279 *         cross check depends on the instruction
                                                    280 *
0000035E  D207 5050 84D0         00000050  000006D0 281           MVC   SKIPXC,=CL8'          '
00000364  D507 5010 84D8         00000010  000006D8 282           CLC   OPNAME,=CL8'VCNF'
0000036A  4780 8194                        00000394 283           BE    XCVCNF
                                                    284
0000036E  D507 5010 84E0         00000010  000006E0 285           CLC   OPNAME,=CL8'VCLFNH'
00000374  4780 81C8                        000003C8 286           BE    XCVCLFNH
                                                    287
00000378  D507 5010 84E8         00000010  000006E8 288           CLC   OPNAME,=CL8'VCFN'
0000037E  4780 81FC                        000003FC 289           BE    XCVCFN
                                                    290
00000382  D507 5010 84F0         00000010  000006F0 291           CLC   OPNAME,=CL8'VCLFNL'
00000388  4780 8230                        00000430 292           BE    XCVCLFNL
                                                    293
0000038C  D207 5050 84C8         00000050  000006C8 294           MVC   SKIPXC,=CL8'SKIP XC '
00000392  07FF                                      295           BR    R15                     return from xcheck
                                                    296
                                                    297 * cross check: VCNF     - VECTOR FP CONVERT TO NNP
                                                    298 *
00000394                                            299 XCVCNF   DS    0F
00000394  B29D 84C4                        000006C4 300           LFPC  FPCINIT                 initialize FPC
                                                    301
00000398  E700 5028 0806                   00000028 302           VL    V16,V1OUTPUT
0000039E  E6F0 0000 145D                            303           VCFN  V15,V16,1,0
000003A4  B29C 5078                        00000078 304           STFPC FPC_XC                  save FPC
000003A8  E7F0 5060 000E                   00000060 305           VST   V15,XCOUTPUT
                                                    306
000003AE  9500 507A                        0000007A 307           CLI   FPC_XC+2,0
000003B2  477F 0000                        00000000 308           BNZ   0(R15)                  some VXC error , so exit
                                                    309
000003B6  E310 500C 0014                   0000000C 310           LGF   R1,V2ADDR               expected source address
000003BC  D50F 5060 1000         00000060  00000000 311           CLC   XCOUTPUT,0(R1)
000003C2  4770 8264                        00000464 312           BNE   XCFAILMSG
000003C6  07FF                                      313           BR    R15                     return from xcheck
                                                    314
                                                    315 * cross check: VCLFNH   - VECTOR FP CONVERT AND LENGTHEN FROM NNP HIGH
                                                    316 *
000003C8                                            317 XCVCLFNH DS    0F
000003C8  B29D 84C4                        000006C4 318           LFPC  FPCINIT                 initialize FPC
                                                    319
000003CC  E700 5028 0806                   00000028 320           VL    V16,V1OUTPUT
000003D2  E6F0 0002 0675                            321           VCRNF V15,V16,V16,0,2
000003D8  B29C 5078                        00000078 322           STFPC FPC_XC                  save FPC
000003DC  E7F0 5060 000E                   00000060 323           VST   V15,XCOUTPUT
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     324
000003E2  9500 507A                      0000007A   325          CLI   FPC_XC+2,0
000003E6  477F 0000                      00000000   326          BNZ   0(R15)                 some VXC error , so exit
                                                     327
000003EA  E310 500C 0014                 0000000C   328          LGF   R1,V2ADDR              expected source address
000003F0  D507 5060 1000                 00000000   329          CLC   XCOUTPUT(8),0(R1)
000003F6  4770 8264                      00000464   330          BNE   XCFAILMSG
000003FA  07FF                                      331          BR    R15                    return from xcheck
                                                     332
                                                     333 * cross check: VCFN     - VECTOR FP CONVERT FROM NNP
                                                     334 *
000003FC                                             335 XCVCFN   DS    0F
000003FC  B29D 84C4                      000006C4   336          LFPC  FPCINIT                initialize FPC
                                                     337
00000400  E700 5028 0806                 00000028   338          VL    V16,V1OUTPUT
00000406  E6F0 0001 0455                            339          VCNF  V15,V16,0,1
0000040C  B29C 5078                      00000078   340          STFPC FPC_XC                 save FPC
00000410  E7F0 5060 000E                 00000060   341          VST   V15,XCOUTPUT
                                                     342
00000416  9500 507A                      0000007A   343          CLI   FPC_XC+2,0
0000041A  477F 0000                      00000000   344          BNZ   0(R15)                 some VXC error , so exit
                                                     345
0000041E  E310 500C 0014                 0000000C   346          LGF   R1,V2ADDR              expected source address
00000424  D50F 5060 1000      00000060   00000000   347          CLC   XCOUTPUT,0(R1)
0000042A  4770 8264                      00000464   348          BNE   XCFAILMSG
0000042E  07FF                                      349          BR    R15                    return from xcheck
                                                     350
                                                     351 * cross check: VCLFNL   - VECTOR FP CONVERT AND LENGTHEN FROM NNP LOW
                                                     352 *
00000430                                             353 XCVCLFNL DS    0F
00000430  B29D 84C4                      000006C4   354          LFPC  FPCINIT                initialize FPC
                                                     355
00000434  E700 5028 0806                 00000028   356          VL    V16,V1OUTPUT
0000043A  E6F0 0002 0675                            357          VCRNF V15,V16,V16,0,2
00000440  B29C 5078                      00000078   358          STFPC FPC_XC                 save FPC
00000444  E7F0 5060 000E                 00000060   359          VST   V15,XCOUTPUT
                                                     360
0000044A  9500 507A                      0000007A   361          CLI   FPC_XC+2,0
0000044E  477F 0000                      00000000   362          BNZ   0(R15)                 some VXC error , so exit
                                                     363
00000452  E310 500C 0014                 0000000C   364          LGF   R1,V2ADDR              expected source address
00000458  D507 5060 1008                 00000008   365          CLC   XCOUTPUT(8),8(R1)         low part of vector
0000045E  4770 8264                      00000464   366          BNE   XCFAILMSG
00000462  07FF                                      367          BR    R15                    return from xcheck
                                                     368
                                                     369
                                                     370 * xcheck failed message
00000464                                             371 XCFAILMSG DS   0H
00000464  4820 5004                      00000004   372          LH    R2,TNUM                get test number and convert
00000468  4E20 8ECA                      000010CA   373          CVD   R2,DECNUM
0000046C  D211 8EB4 8E9E      000010B4   0000109E   374          MVC   PRT3,EDIT
00000472  DE11 8EB4 8ECA      000010B4   000010CA   375          ED    PRT3,DECNUM
00000478  D202 8E5D 8EC1      0000105D   000010C1   376          MVC   XCPTNUM(3),PRT3+13     fill in message with test #
                                                     377
0000047E  D207 8E7F 5010      0000107F   00000010   378          MVC   XCPNAME,OPNAME         fill in message with instruction
                                                     379
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00000484  B982 0022                          380           XGR   R2,R2
00000488  4320 5008                00000008  381           IC    R2,M3                get m3 and convert
0000048C  4E20 8ECA                000010CA  382           CVD   R2,DECNUM
00000490  D211 8EB4 8E9E      000010B4 0000109E  383           MVC   PRT3,EDIT
00000496  DE11 8EB4 8ECA      000010B4 000010CA  384           ED    PRT3,DECNUM
0000049C  D201 8E90 8EC2      00001090 000010C2  385           MVC   XCPM3(2),PRT3+14     fill in message with m3 field
                                                 386 *
000004A2  B982 0022                          387           XGR   R2,R2
000004A6  4320 5009                00000009  388           IC    R2,M4                get m4 and convert
000004AA  4E20 8ECA                000010CA  389           CVD   R2,DECNUM
000004AE  D211 8EB4 8E9E      000010B4 0000109E  390           MVC   PRT3,EDIT
000004B4  DE11 8EB4 8ECA      000010B4 000010CA  391           ED    PRT3,DECNUM
000004BA  D201 8E9B 8EC2      0000109B 000010C2  392           MVC   XCPM4(2),PRT3+14     fill in message with m4 field
                                                 393
000004C0  50F0 8310                00000510  394           ST    R15,XCR15            save r15
000004C4  4100 004E                0000004E  395           LA    R0,XCPLNG            message length
000004C8  4110 8E50                00001050  396           LA    R1,XCPLINE           messagfe address
000004CC  45F0 839E                0000059E  397           BAL   R15,RPTERROR
000004D0  58F0 8310                00000510  398           L     R15,XCR15
                                                 399
000004D4  5800 8504                00000704  400           L     R0,=F'1'             set failed test indicator
000004D8  5000 8E00                00001000  401           ST    R0,FAILED
000004DC  07FF                               402           BR    R15                  return from xcheck
                                                 403
000004E0                                     404           DS    0FD
000004E0  00000000 00000000                  405 XCRESULT  DS    XL16
000004F0  00000000 00000000                  406 XCV1      DS    XL16
00000500  00000000 00000000                  407 XCV2      DS    XL16
00000510  00000000 00000000                  408 XCR15     DS    FD
                                                 409
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    411 ************************************************************************
                                                    412 * result not as expected:
                                                    413 *        issue message with test number, instruction under test
                                                    414 *              and instruction m4
                                                    415 ************************************************************************
                                 00000518  00000001   416 FAILMSG  EQU   *
00000518  4820 5004                        00000004   417          LH    R2,TNUM              get test number and convert
0000051C  4E20 8ECA                        000010CA   418          CVD   R2,DECNUM
00000520  D211 8EB4 8E9E       000010B4    0000109E   419          MVC   PRT3,EDIT
00000526  DE11 8EB4 8ECA       000010B4    000010CA   420          ED    PRT3,DECNUM
0000052C  D202 8E15 8EC1       00001015    000010C1   421          MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                    422
00000532  D207 8E30 5010       00001030    00000010   423          MVC   PRTNAME,OPNAME       fill in message with instruction
                                                    424 *
00000538  B982 0022                                 425          XGR   R2,R2
0000053C  4320 5008                        00000008   426          IC    R2,M3                get m3 and convert
00000540  4E20 8ECA                        000010CA   427          CVD   R2,DECNUM
00000544  D211 8EB4 8E9E       000010B4    0000109E   428          MVC   PRT3,EDIT
0000054A  DE11 8EB4 8ECA       000010B4    000010CA   429          ED    PRT3,DECNUM
00000550  D201 8E41 8EC2       00001041    000010C2   430          MVC   PRTM3(2),PRT3+14     fill in message with m3 field
                                                    431 *
00000556  B982 0022                                 432          XGR   R2,R2
0000055A  4320 5009                        00000009   433          IC    R2,M4                get m4 and convert
0000055E  4E20 8ECA                        000010CA   434          CVD   R2,DECNUM
00000562  D211 8EB4 8E9E       000010B4    0000109E   435          MVC   PRT3,EDIT
00000568  DE11 8EB4 8ECA       000010B4    000010CA   436          ED    PRT3,DECNUM
0000056E  D201 8E4D 8EC2       0000104D    000010C2   437          MVC   PRTM4(2),PRT3+14     fill in message with m4 field
                                                    438 *
00000574  4100 0048                        00000048   439          LA    R0,PRTLNG            message length
00000578  4110 8E08                        00001008   440          LA    R1,PRTLINE           messagfe address
0000057C  45F0 839E                        0000059E   441          BAL   R15,RPTERROR


                                                    443 ************************************************************************
                                                    444 * continue after a failed test
                                                    445 ************************************************************************
                                 00000580  00000001   446 FAILCONT EQU   *
00000580  5800 8504                        00000704   447          L     R0,=F'1'             set failed test indicator
00000584  5000 8E00                        00001000   448          ST    R0,FAILED
                                                    449
00000588  41C0 C004                        00000004   450          LA    R12,4(0,R12)         next test address
0000058C  47F0 80EC                        000002EC   451          B     NEXTE6


                                                    453 ************************************************************************
                                                    454 * end of testing; set ending psw
                                                    455 ************************************************************************
                                 00000590  00000001   456 ENDTEST  EQU   *
00000590  5810 8E00                        00001000   457          L     R1,FAILED            did a test fail?
00000594  1211                                      458          LTR   R1,R1
00000596  4780 84A0                        000006A0   459          BZ    EOJ                     No, exit
0000059A  47F0 84B8                        000006B8   460          B     FAILTEST                Yes, exit with BAD PSW
                                                    461
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    463 ************************************************************************
                                                    464 *        RPTERROR          Report instruction test in error
                                                    465 *                             R0 = MESSGAE LENGTH
                                                    466 *                             R1 = ADDRESS OF MESSAGE
                                                    467 ************************************************************************

0000059E  50F0 83BC                 000005BC    469 RPTERROR ST    R15,RPTSAVE          Save return address
000005A2  5050 83C0                 000005C0    470          ST    R5,RPTSVR5           Save R5
                                                    471 *
                                                    472 *        Use Hercules Diagnose for Message to console
                                                    473 *
000005A6  9002 83C8                 000005C8    474          STM   R0,R2,RPTDWSAV       save regs used by MSG
000005AA  4520 83D8                 000005D8    475          BAL   R2,MSG               call Hercules console MSG display
000005AE  9802 83C8                 000005C8    476          LM    R0,R2,RPTDWSAV       restore regs


000005B2  5850 83C0                 000005C0    478          L     R5,RPTSVR5           Restore R5
000005B6  58F0 83BC                 000005BC    479          L     R15,RPTSAVE          Restore return address
000005BA  07FF                                  480          BR    R15                  Return to caller

000005BC  00000000                              482 RPTSAVE  DC    F'0'                 R15 save area
000005C0  00000000                              483 RPTSVR5  DC    F'0'                 R5 save area

000005C8  00000000 00000000                     485 RPTDWSAV DC    2D'0'                R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    487 ************************************************************************
                                                    488 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                    489 *              R2 = return address
                                                    490 ************************************************************************
000005D8  4900 8508                         00000708   492 MSG      CH    R0,=H'0'                Do we even HAVE a message?
000005DC  07D2                                         493          BNHR  R2                      No, ignore

000005DE  9002 8414                         00000614   495          STM   R0,R2,MSGSAVE           Save registers

000005E2  4900 850A                         0000070A   497          CH    R0,=AL2(L'MSGMSG)       Message length within limits?
000005E6  47D0 83EE                         000005EE   498          BNH   MSGOK                   Yes, continue
000005EA  4100 005F                         0000005F   499          LA    R0,L'MSGMSG             No, set to maximum

000005EE  1820                                         501 MSGOK    LR    R2,R0                   Copy length to work register
000005F0  0620                                         502          BCTR  R2,0                    Minus-1 for execute
000005F2  4420 8420                         00000620   503          EX    R2,MSGMVC               Copy message to O/P buffer

000005F6  4120 200A                         0000000A   505          LA    R2,1+L'MSGCMD(,R2)      Calculate true command length
000005FA  4110 8426                         00000626   506          LA    R1,MSGCMD               Point to true command

000005FE  83120008                                     508          DC    X'83',X'12',X'0008'     Issue Hercules Diagnose X'008'
00000602  4780 840E                         0000060E   509          BZ    MSGRET                  Return if successful
                                                       510
00000606  1222                                         511          LTR   R2,R2                   Is Diag8 Ry (R2) 0?
00000608  4780 840E                         0000060E   512          BZ    MSGRET                    an error occurred but coninue
                                                       513
0000060C  0000                                         514          DC    H'0'                    CRASH for debugging purposes

0000060E  9802 8414                         00000614   516 MSGRET   LM    R0,R2,MSGSAVE           Restore registers
00000612  07F2                                         517          BR    R2                      Return to caller

00000614  00000000 00000000                            519 MSGSAVE  DC    3F'0'                   Registers save area
00000620  D200 842F 1000       0000062F   00000000     520 MSGMVC   MVC   MSGMSG(0),0(R1)         Executed instruction

00000626  D4E2C7D5 D6C8405C                            522 MSGCMD   DC    C'MSGNOH * '            *** HERCULES MESSAGE COMMAND ***
0000062F  40404040 40404040                            523 MSGMSG   DC    CL95' '                 The message text to be displayed
                                                       524
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      526 ************************************************************************
                                                      527 *        Normal completion or Abnormal termination PSWs
                                                      528 ************************************************************************

00000690  00020001 80000000                           530 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)
000006A0  B2B2 8490                   00000690        532 EOJ      LPSWE EOJPSW               Normal completion

000006A8  00020001 80000000                           534 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')
000006B8  B2B2 84A8                   000006A8        536 FAILTEST LPSWE FAILPSW              Abnormal termination

                                                      538 ************************************************************************
                                                      539 *        Working Storage
                                                      540 ************************************************************************

000006BC  00000000                                    542 CTLR0    DS    F                    CR0
000006C0  00000000                                    543          DS    F
000006C4  00000000                                    544 FPCINIT  DC    XL4'00000000'        FPC before test

                                                      546
000006C8                                              547          LTORG ,                    Literals pool
000006C8  E2D2C9D7 40E7C340                           548                =CL8'SKIP XC '
000006D0  40404040 40404040                           549                =CL8'        '
000006D8  E5C3D5C6 40404040                           550                =CL8'VCNF'
000006E0  E5C3D3C6 D5C84040                           551                =CL8'VCLFNH'
000006E8  E5C3C6D5 40404040                           552                =CL8'VCFN'
000006F0  E5C3D3C6 D5D34040                           553                =CL8'VCLFNL'
000006F8  00000004                                    554                =F'4'
000006FC  000038CC                                    555                =A(E6TESTS)
00000700  00000008                                    556                =XL4'00000008'
00000704  00000001                                    557                =F'1'
00000708  0000                                        558                =H'0'
0000070A  005F                                        559                =AL2(L'MSGMSG)
0000070C  E2                                          560                =CL1'S'
                                                      561
                                                      562 *        some constants
                                                      563
                          00000400  00000001          564 K        EQU   1024               One KB
                          00001000  00000001          565 PAGE     EQU   (4*K)              Size of one page
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                             00010000  00000001    566 K64      EQU   (64*K)           64 KB
                             00100000  00000001    567 MB       EQU   (K*K)             1 MB
                                                   568
                                                   569
                             AABBCCDD  00000001    570 REG2PATT EQU   X'AABBCCDD'    Polluted Register pattern
                             000000DD  00000001    571 REG2LOW  EQU         X'DD'    (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     573 *=====================================================================
                                                     574 *
                                                     575 *  NOTE: start data on an address that is easy to display
                                                     576 *        within Hercules
                                                     577 *
                                                     578 *=====================================================================
                                                     579
0000070D                      0000070D  00001000     580          ORG   ZVE6TST+X'1000'
00001000  00000000                                   581 FAILED   DC    F'0'                    some test failed?
00001004  00000000                                   582 TESTING  DC    F'0'                    current test #

                                                     584 ***************************************************************************
                                                     585 *        TEST failed : result messgae
                                                     586 ***************************************************************************
                                                     587 *
                                                     588 *        failed message and associated editting
                                                     589 *
00001008  40404040 4040E385                          590 PRTLINE  DC    C'      Test # '
00001015  A7A7A7                                     591 PRTNUM   DC    C'xxx'
00001018  40868189 93858440                          592          DC    c' failed for instruction '
00001030  A7A7A7A7 A7A7A7A7                          593 PRTNAME  DC    CL8'xxxxxxxx'
00001038  40A689A3 884094F3                          594          DC    C' with m3='
00001041  A7A7                                       595 PRTM3    DC    C'xx'
00001043  6B                                         596          DC    C','
00001044  40A689A3 884094F4                          597          DC    C' with m4='
0000104D  A7A7                                       598 PRTM4    DC    C'xx'
0000104F  4B                                         599          DC    C'.'
                                00000048  00000001   600 PRTLNG   EQU   *-PRTLINE


                                                     602 ***************************************************************************
                                                     603 *        TEST failed : XCHECK
                                                     604 ***************************************************************************
                                                     605 *
                                                     606 *        XCHECK failed message
                                                     607 *
00001050  40404040 4040E385                          608 XCPLINE  DC    C'      Test # '
0000105D  A7A7A7                                     609 XCPTNUM  DC    C'xxx'
00001060  40E7C3C8 C5C3D240                          610          DC    c' XCHECK failed for instruction '
0000107F  A7A7A7A7 A7A7A7A7                          611 XCPNAME  DC    CL8'xxxxxxxx'
00001087  40A689A3 884094F3                          612          DC    C' with m3='
00001090  A7A7                                       613 XCPM3    DC    C'xx'
00001092  40A689A3 884094F4                          614          DC    C' with m4='
0000109B  A7A7                                       615 XCPM4    DC    C'xx'
0000109D  4B                                         616          DC    C'.'
                                0000004E  00000001   617 XCPLNG   EQU   *-XCPLINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                     619 ************************************************************************
                                                     620 *        TEST failed : message working storge
                                                     621 ************************************************************************
0000109E  40212020 20202020                          622 EDIT     DC    XL18'40212020202020202020202020202020'
                                                     623
000010B0  7E7E7E6E                                   624          DC    C'===>'
000010B4  40404040 40404040                          625 PRT3     DC    CL18' '
000010C6  4C7E7E7E                                   626          DC    C'<==='
000010CA  00000000 00000000                          627 DECNUM   DS    CL16


                                                     629 *
                                                     630 *        Vector instruction results, pollution and input
                                                     631 *
000010DA  00000000 00000000                          632          DS    XL16                                        gap
000010EA  FFFFFFFF FFFFFFFF                          633 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
000010FA  12345678 90123456                          634 V1INPUT  DC    XL16'1234567890123456789012345678901D'    V1 input
0000110A  00000000 00000000                          635          DS    XL16
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     637 ********************************************************************************
                                                     638 *        E6TEST DSECT
                                                     639 ********************************************************************************


                                                     641 E6TEST   DSECT ,
00000000  00000000                                   642 TSUB     DC    A(0)              pointer  to test
00000004  0000                                       643 TNUM     DC    H'00'             Test Number
00000006  00                                         644          DC    X'00'
00000007  40                                         645 XCSKIP   DC    CL1' '            Y = skip cross check
00000008  00                                         646 M3       DC    HL1'00'           m3 used
00000009  00                                         647 M4       DC    HL1'00'           m4 used
0000000A  00                                         648 FLG      DC    X'00'             expected FPC flags
0000000B  00                                         649 VXC      DC    X'00'             VXC expected
0000000C  00000000                                   650 V2ADDR   DC    A(0)              address of v2: 16-byte packed decimal
00000010  40404040 40404040                          651 OPNAME   DC    CL8' '            E6 name
00000018  00000000                                   652 RELEN    DC    A(0)              result length
0000001C  00000000                                   653 READDR   DC    A(0)              expected result address
00000020  00000000 00000000                          654          DS    FD                   gap
00000028  00000000 00000000                          655 V1OUTPUT DS    XL16              V1 Output
00000038  00000000 00000000                          656          DS    FD                   gap
00000040  00000000                                   657 FPC_R    DS    F                 FPC after instruction
00000048  00000000 00000000                          658          DS    FD                   gap
00000050  40404040 40404040                          659 SKIPXC   DC    CL8' '            was cross check skipped?
00000058  00000000 00000000                          660          DS    FD                   gap
00000060  00000000 00000000                          661 XCOUTPUT DS    XL16              Cross check Output
00000070  00000000 00000000                          662          DS    FD                   gap
00000078  00000000                                   663 FPC_XC   DS    F                 FPC after cross check
00000080  00000000 00000000                          664          DS    FD                   gap
00000088  00000000                                   665 WK1      DS    F                 debug area
0000008C  00000000                                   666 WK2      DS    F
00000090                                             667          DS    0F
                                                     668 **
                                                     669 *        test routine will be here (from VRR-a macro)


                          00000000  00003997         671 ZVE6TST  CSECT ,
0000111C                                             672          DS    0F


                                                     674 ********************************************************************************
                                                     675 *     Macros to help build test tables
                                                     676 ********************************************************************************


                                                     678 *
                                                     679 * macro to generate individual test
                                                     680 *
                                                     681          MACRO
                                                     682          VRR_A &INST,&M3,&M4,&FLAGS,&VXC,&SKIP
                                                     683 .*                                 &INST  - VRR-a instruction under test
                                                     684 .*                                 &m3    - m3 field
                                                     685 .*                                 &m4    - m4 field
                                                     686 .*                                 &flags - expected FPC flags
                                                     687 .*                                 &VXC   - expected VXC
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   688 .*                                  &SKIP  - S = skip cross check
                                                   689          GBLA  &TNUM
                                                   690 &TNUM    SETA  &TNUM+1
                                                   691
                                                   692          DS    0FD
                                                   693          USING *,R5                 base for test data and test routine
                                                   694
                                                   695 T&TNUM   DC    A(X&TNUM)          address of test routine
                                                   696          DC    H'&TNUM'           test number
                                                   697          DC    X'00'
                                                   698          DC    CL1'&SKIP'         Y = skip cross check
                                                   699          DC    HL1'&M3'           m3
                                                   700          DC    HL1'&M4'           m4
                                                   701 FLG&TNUM DC    X'&FLAGS'          expected FPC flags
                                                   702 VXC&TNUM DC    X'&VXC'            expected VXC
                                                   703 V2_&TNUM DC    A(RE&TNUM+16)      address of v2: 16-byte packed decimal
                                                   704          DC    CL8'&INST'         instruction name
                                                   705          DC    A(16)              result length
                                                   706          DC    A(RE&TNUM)         address of expected resul
                                                   707          DS    FD                 gap
                                                   708 V1O&TNUM DS    XL16               V1 output
                                                   709          DS    FD                    gap
                                                   710 FPC_R_&TNUM DS F                  FPC after instruction
                                                   711          DS    FD                    gap
                                                   712          DC    CL8' '             was cross check skipped?
                                                   713          DS    FD                    gap
                                                   714 XCO&TNUM DS    XL16               Cross check Output
                                                   715          DS    FD                    gap
                                                   716 FPC_XC_&TNUM DS F                 FPC after cross check
                                                   717          DS    FD                    gap
                                                   718          DS    F                  debug area
                                                   719          DS    F
                                                   720 .*
                                                   721 *
                                                   722 X&TNUM   DS    0F
                                                   723          LFPC  FPCINIT            initialize FPC
                                                   724
                                                   725          LGF   R2,V2_&TNUM        get v2
                                                   726          VL    V22,0(R2)
                                                   727
                                                   728          &INST V22,V22,&M3,&M4    test instruction (dest is source)
                                                   729
                                                   730          STFPC FPC_R_&TNUM        save FPC
                                                   731          VST   V22,V1O&TNUM       save instruction result
                                                   732
                                                   733          BR    R11                return
                                                   734
                                                   735 RE&TNUM  DS    0F                 expected 16 byte result
                                                   736          DROP  R5
                                                   737
                                                   738          MEND


                                                   740 *
                                                   741 * macro to generate table of pointers to individual tests
```

```
 LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                    742 *
                                                    743          MACRO
                                                    744          PTTABLE
                                                    745          GBLA  &TNUM
                                                    746          LCLA  &CUR
                                                    747 &CUR     SETA  1
                                                    748 .*
                                                    749 TTABLE   DS    0F
                                                    750 .LOOP    ANOP
                                                    751 .*
                                                    752          DC    A(T&CUR)           TEST &CUR
                                                    753 .*
                                                    754 &CUR     SETA  &CUR+1
                                                    755          AIF   (&CUR LE &TNUM).LOOP
                                                    756 *
                                                    757          DC    A(0)               END OF TABLE
                                                    758          DC    A(0)
                                                    759 .*
                                                    760          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     762 ************************************************************************
                                                     763 *        E6 VRR-a tests
                                                     764 ************************************************************************
                                                     765          PRINT DATA
                                                     766 *
                                                     767 *        E655 VCNF     - VECTOR FP CONVERT TO NNP
                                                     768 *        E656 VCLFNH   - VECTOR FP CONVERT AND LENGTHEN FROM NNP HIGH
                                                     769 *        E65D VCFN     - VECTOR FP CONVERT FROM NNP
                                                     770 *        E65E VCLFNL   - VECTOR FP CONVERT AND LENGTHEN FROM NNP LOW
                                                     771 *
                                                     772 *------------------------------------------------------------------
                                                     773 *   VRR-a   instruction, m3, m4, flags, VXC, SKIP
                                                     774 *   followed by
                                                     775 *              followed by
                                                     776 *              v1 - 16 byte expected result
                                                     777 *              v2 - 16 byte source
                                                     778 *------------------------------------------------------------------
                                                     779 * VCNF     - VECTOR FP CONVERT TO NNP
                                                     780 *------------------------------------------------------------------
                                                     781 * tinyb -> dlfloat  (with cross check dlfloat -> tinyb)
                                                     782 *
                                                     783 * some of these tests use numbers from PoP SA22-7832-13,
                                                     784 * Figure 9-2. Examples of Floating-Point Numbers ( page 9-6 )
                                                     785 *
                                                     786 * +0     simple instruction test and 'test' test
                                                     787          VRR_A VCNF,0,1,00,00,N
00001120                                             788+         DS    0FD
00001120                          00001120           789+         USING *,R5              base for test data and test routine
00001120  000011B0                                   790+T1       DC    A(X1)             address of test routine
00001124  0001                                       791+         DC    H'1'              test number
00001126  00                                         792+         DC    X'00'
00001127  D5                                         793+         DC    CL1'N'            Y = skip cross check
00001128  00                                         794+         DC    HL1'0'            m3
00001129  01                                         795+         DC    HL1'1'            m4
0000112A  00                                         796+FLG1     DC    X'00'             expected FPC flags
0000112B  00                                         797+VXC1     DC    X'00'             expected VXC
0000112C  000011E4                                   798+V2_1     DC    A(RE1+16)         address of v2: 16-byte packed decimal
00001130  E5C3D5C6 40404040                          799+         DC    CL8'VCNF'         instruction name
00001138  00000010                                   800+         DC    A(16)             result length
0000113C  000011D4                                   801+         DC    A(RE1)            address of expected resul
00001140  00000000 00000000                          802+         DS    FD                gap
00001148  00000000 00000000                          803+V1O1     DS    XL16              V1 output
00001150  00000000 00000000
00001158  00000000 00000000                          804+         DS    FD                   gap
00001160  00000000                                   805+FPC_R_1  DS    F                 FPC after instruction
00001168  00000000 00000000                          806+         DS    FD                   gap
00001170  40404040 40404040                          807+         DC    CL8' '            was cross check skipped?
00001178  00000000 00000000                          808+         DS    FD                   gap
00001180  00000000 00000000                          809+XCO1     DS    XL16              Cross check Output
00001188  00000000 00000000
00001190  00000000 00000000                          810+         DS    FD                   gap
00001198  00000000                                   811+FPC_XC_1 DS    F                 FPC after cross check
000011A0  00000000 00000000                          812+         DS    FD                   gap
000011A8  00000000                                   813+         DS    F                 debug area
000011AC  00000000                                   814+         DS    F
                                                     815+*
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000011B0                                          816+X1       DS    0F
000011B0  B29D 84C4                     000006C4  817+         LFPC  FPCINIT           initialize FPC
000011B4  E320 500C 0014                0000112C  818+         LGF   R2,V2_1           get v2
000011BA  E762 0000 0806                00000000  819+         VL    V22,0(R2)
000011C0  E666 0001 0C55                          820+         VCNF  V22,V22,0,1       test instruction (dest is source)
000011C6  B29C 5040                     00001160  821+         STFPC FPC_R_1           save FPC
000011CA  E760 5028 080E                00001148  822+         VST   V22,V1O1          save instruction result
000011D0  07FB                                    823+         BR    R11               return
000011D4                                          824+RE1      DS    0F                expected 16 byte result
000011D4                                          825+         DROP  R5
000011D4  00000000 00000000                       826          DC    XL16'00000000000000000000000000000000'
000011DC  00000000 00000000
000011E4  00000000 00000000                       827          DC    XL16'00000000000000000000000000000000'
000011EC  00000000 00000000
                                                  828
                                                  829 * 1.0, -1
                                                  830          VRR_A VCNF,0,1,00,00,N
000011F8                                          831+         DS    0FD
000011F8                        000011F8          832+         USING *,R5              base for test data and test routine
000011F8  00001288                                833+T2       DC    A(X2)             address of test routine
000011FC  0002                                    834+         DC    H'2'              test number
000011FE  00                                      835+         DC    X'00'
000011FF  D5                                      836+         DC    CL1'N'            Y = skip cross check
00001200  00                                      837+         DC    HL1'0'            m3
00001201  01                                      838+         DC    HL1'1'            m4
00001202  00                                      839+FLG2     DC    X'00'             expected FPC flags
00001203  00                                      840+VXC2     DC    X'00'             expected VXC
00001204  000012BC                                841+V2_2     DC    A(RE2+16)         address of v2: 16-byte packed decimal
00001208  E5C3D5C6 40404040                       842+         DC    CL8'VCNF'         instruction name
00001210  00000010                                843+         DC    A(16)             result length
00001214  000012AC                                844+         DC    A(RE2)            address of expected resul
00001218  00000000 00000000                       845+         DS    FD                gap
00001220  00000000 00000000                       846+V1O2     DS    XL16              V1 output
00001228  00000000 00000000
00001230  00000000 00000000                       847+         DS    FD                   gap
00001238  00000000                                848+FPC_R_2  DS    F                 FPC after instruction
00001240  00000000 00000000                       849+         DS    FD                   gap
00001248  40404040 40404040                       850+         DC    CL8' '            was cross check skipped?
00001250  00000000 00000000                       851+         DS    FD                   gap
00001258  00000000 00000000                       852+XCO2     DS    XL16              Cross check Output
00001260  00000000 00000000
00001268  00000000 00000000                       853+         DS    FD                   gap
00001270  00000000                                854+FPC_XC_2 DS    F                 FPC after cross check
00001278  00000000 00000000                       855+         DS    FD                   gap
00001280  00000000                                856+         DS    F                 debug area
00001284  00000000                                857+         DS    F
                                                  858+*
00001288                                          859+X2       DS    0F
00001288  B29D 84C4                     000006C4  860+         LFPC  FPCINIT           initialize FPC
0000128C  E320 9004 0014                00001204  861+         LGF   R2,V2_2           get v2
00001292  E762 0000 0806                00000000  862+         VL    V22,0(R2)
00001298  E666 0001 0C55                          863+         VCNF  V22,V22,0,1       test instruction (dest is source)
0000129E  B29C 9038                     00001238  864+         STFPC FPC_R_2           save FPC
000012A2  E760 9020 080E                00001220  865+         VST   V22,V1O2          save instruction result
000012A8  07FB                                    866+         BR    R11               return
000012AC                                          867+RE2      DS    0F                expected 16 byte result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000012AC                                           868+         DROP  R5
000012AC  3E000000 BE000000                        869          DC    XL16'3E000000BE000000000000000000D800'
000012B4  00000000 0000D800
000012BC  3C000000 BC000000                        870          DC    XL16'3C000000BC000000000000000000F000'
000012C4  00000000 0000F000
                                                   871 * 0.5
                                                   872          VRR_A VCNF,0,1,00,00,N
000012D0                                           873+         DS    0FD
000012D0                      000012D0             874+         USING *,R5              base for test data and test routine
000012D0  00001360                                 875+T3       DC    A(X3)             address of test routine
000012D4  0003                                     876+         DC    H'3'              test number
000012D6  00                                       877+         DC    X'00'
000012D7  D5                                       878+         DC    CL1'N'            Y = skip cross check
000012D8  00                                       879+         DC    HL1'0'            m3
000012D9  01                                       880+         DC    HL1'1'            m4
000012DA  00                                       881+FLG3     DC    X'00'             expected FPC flags
000012DB  00                                       882+VXC3     DC    X'00'             expected VXC
000012DC  00001394                                 883+V2_3     DC    A(RE3+16)         address of v2: 16-byte packed decimal
000012E0  E5C3D5C6 40404040                        884+         DC    CL8'VCNF'         instruction name
000012E8  00000010                                 885+         DC    A(16)             result length
000012EC  00001384                                 886+         DC    A(RE3)            address of expected resul
000012F0  00000000 00000000                        887+         DS    FD                gap
000012F8  00000000 00000000                        888+V1O3     DS    XL16              V1 output
00001300  00000000 00000000
00001308  00000000 00000000                        889+         DS    FD                   gap
00001310  00000000                                 890+FPC_R_3  DS    F                 FPC after instruction
00001318  00000000 00000000                        891+         DS    FD                   gap
00001320  40404040 40404040                        892+         DC    CL8' '            was cross check skipped?
00001328  00000000 00000000                        893+         DS    FD                   gap
00001330  00000000 00000000                        894+XCO3     DS    XL16              Cross check Output
00001338  00000000 00000000
00001340  00000000 00000000                        895+         DS    FD                   gap
00001348  00000000                                 896+FPC_XC_3 DS    F                 FPC after cross check
00001350  00000000 00000000                        897+         DS    FD                   gap
00001358  00000000                                 898+         DS    F                 debug area
0000135C  00000000                                 899+         DS    F
                                                   900+*
00001360                                           901+X3       DS    0F
00001360  B29D 84C4                    000006C4    902+         LFPC  FPCINIT           initialize FPC
00001364  E320 500C 0014               000012DC    903+         LGF   R2,V2_3           get v2
0000136A  E762 0000 0806               00000000    904+         VL    V22,0(R2)
00001370  E666 0001 0C55                           905+         VCNF  V22,V22,0,1       test instruction (dest is source)
00001376  B29C 5040                    00001310    906+         STFPC FPC_R_3           save FPC
0000137A  E760 5028 080E               000012F8    907+         VST   V22,V1O3          save instruction result
00001380  07FB                                     908+         BR    R11               return
00001384                                           909+RE3      DS    0F                expected 16 byte result
00001384                                           910+         DROP  R5
00001384  3C000000 00000000                        911          DC    XL16'3C0000000000000000000000000D800'
0000138C  00000000 0000D800
00001394  38000000 00000000                        912          DC    XL16'380000000000000000000000000F000'
0000139C  00000000 0000F000
                                                   913
                                                   914 * 1/64
                                                   915          VRR_A VCNF,0,1,00,00,N
000013A8                                           916+         DS    0FD
000013A8                      000013A8             917+         USING *,R5              base for test data and test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000013A8  00001438                            918+T4       DC    A(X4)             address of test routine
000013AC  0004                                919+         DC    H'4'              test number
000013AE  00                                  920+         DC    X'00'
000013AF  D5                                  921+         DC    CL1'N'            Y = skip cross check
000013B0  00                                  922+         DC    HL1'0'            m3
000013B1  01                                  923+         DC    HL1'1'            m4
000013B2  00                                  924+FLG4     DC    X'00'             expected FPC flags
000013B3  00                                  925+VXC4     DC    X'00'             expected VXC
000013B4  0000146C                            926+V2_4     DC    A(RE4+16)         address of v2: 16-byte packed decimal
000013B8  E5C3D5C6 40404040                   927+         DC    CL8'VCNF'         instruction name
000013C0  00000010                            928+         DC    A(16)             result length
000013C4  0000145C                            929+         DC    A(RE4)            address of expected resul
000013C8  00000000 00000000                   930+         DS    FD                gap
000013D0  00000000 00000000                   931+V1O4     DS    XL16              V1 output
000013D8  00000000 00000000
000013E0  00000000 00000000                   932+         DS    FD                   gap
000013E8  00000000                            933+FPC_R_4  DS    F                 FPC after instruction
000013F0  00000000 00000000                   934+         DS    FD                   gap
000013F8  40404040 40404040                   935+         DC    CL8' '            was cross check skipped?
00001400  00000000 00000000                   936+         DS    FD                   gap
00001408  00000000 00000000                   937+XCO4     DS    XL16              Cross check Output
00001410  00000000 00000000
00001418  00000000 00000000                   938+         DS    FD                   gap
00001420  00000000                            939+FPC_XC_4 DS    F                 FPC after cross check
00001428  00000000 00000000                   940+         DS    FD                   gap
00001430  00000000                            941+         DS    F                 debug area
00001434  00000000                            942+         DS    F
                                              943+*
00001438                                      944+X4       DS    0F
00001438  B29D 84C4                 000006C4  945+         LFPC  FPCINIT           initialize FPC
0000143C  E320 500C 0014            000013B4  946+         LGF   R2,V2_4           get v2
00001442  E762 0000 0806            00000000  947+         VL    V22,0(R2)
00001448  E666 0001 0C55                      948+         VCNF  V22,V22,0,1       test instruction (dest is source)
0000144E  B29C 5040                 000013E8  949+         STFPC FPC_R_4           save FPC
00001452  E760 5028 080E            000013D0  950+         VST   V22,V1O4          save instruction result
00001458  07FB                                951+         BR    R11               return
0000145C                                      952+RE4      DS    0F                expected 16 byte result
0000145C                                      953+         DROP  R5
0000145C  32000000 00000000                   954          DC    XL16'320000000000000000000000000D800'
00001464  00000000 0000D800
0000146C  24000000 00000000                   955          DC    XL16'240000000000000000000000000F000'
00001474  00000000 0000F000
                                              956
                                              957 * +0, -0
                                              958          VRR_A VCNF,0,1,00,00,N
00001480                                      959+         DS    0FD
00001480                      00001480        960+         USING *,R5              base for test data and test routine
00001480  00001510                            961+T5       DC    A(X5)             address of test routine
00001484  0005                                962+         DC    H'5'              test number
00001486  00                                  963+         DC    X'00'
00001487  D5                                  964+         DC    CL1'N'            Y = skip cross check
00001488  00                                  965+         DC    HL1'0'            m3
00001489  01                                  966+         DC    HL1'1'            m4
0000148A  00                                  967+FLG5     DC    X'00'             expected FPC flags
0000148B  00                                  968+VXC5     DC    X'00'             expected VXC
0000148C  00001544                            969+V2_5     DC    A(RE5+16)         address of v2: 16-byte packed decimal
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
00001490  E5C3D5C6 40404040                        970+          DC    CL8'VCNF'          instruction name
00001498  00000010                                 971+          DC    A(16)              result length
0000149C  00001534                                 972+          DC    A(RE5)             address of expected resul
000014A0  00000000 00000000                        973+          DS    FD                 gap
000014A8  00000000 00000000                        974+V1O5      DS    XL16               V1 output
000014B0  00000000 00000000
000014B8  00000000 00000000                        975+          DS    FD                    gap
000014C0  00000000                                 976+FPC_R_5   DS    F                  FPC after instruction
000014C8  00000000 00000000                        977+          DS    FD                    gap
000014D0  40404040 40404040                        978+          DC    CL8' '             was cross check skipped?
000014D8  00000000 00000000                        979+          DS    FD                    gap
000014E0  00000000 00000000                        980+XCO5      DS    XL16               Cross check Output
000014E8  00000000 00000000
000014F0  00000000 00000000                        981+          DS    FD                    gap
000014F8  00000000                                 982+FPC_XC_5  DS    F                  FPC after cross check
00001500  00000000 00000000                        983+          DS    FD                    gap
00001508  00000000                                 984+          DS    F                  debug area
0000150C  00000000                                 985+          DS    F
                                                   986+*
00001510                                           987+X5        DS    0F
00001510  B29D 84C4                    000006C4    988+          LFPC  FPCINIT            initialize FPC
00001514  E320 500C 0014               0000148C    989+          LGF   R2,V2_5            get v2
0000151A  E762 0000 0806               00000000    990+          VL    V22,0(R2)
00001520  E666 0001 0C55                           991+          VCNF  V22,V22,0,1        test instruction (dest is source)
00001526  B29C 5040                    000014C0    992+          STFPC FPC_R_5            save FPC
0000152A  E760 5028 080E               000014A8    993+          VST   V22,V1O5           save instruction result
00001530  07FB                                     994+          BR    R11                return
00001534                                           995+RE5       DS    0F                 expected 16 byte result
00001534                                           996+          DROP  R5
00001534  00008000 00000000                        997           DC    XL16'00008000000000000000000000000D800'
0000153C  00000000 0000D800
00001544  00008000 00000000                        998           DC    XL16'00008000000000000000000000000F000'
0000154C  00000000 0000F000
                                                   999
                                                  1000 * -15
                                                  1001          VRR_A VCNF,0,1,00,00,N
00001558                                          1002+         DS    0FD
00001558                       00001558           1003+         USING *,R5               base for test data and test routine
00001558  000015E8                                1004+T6       DC    A(X6)              address of test routine
0000155C  0006                                    1005+         DC    H'6'               test number
0000155E  00                                      1006+         DC    X'00'
0000155F  D5                                      1007+         DC    CL1'N'             Y = skip cross check
00001560  00                                      1008+         DC    HL1'0'             m3
00001561  01                                      1009+         DC    HL1'1'             m4
00001562  00                                      1010+FLG6     DC    X'00'              expected FPC flags
00001563  00                                      1011+VXC6     DC    X'00'              expected VXC
00001564  0000161C                                1012+V2_6     DC    A(RE6+16)          address of v2: 16-byte packed decimal
00001568  E5C3D5C6 40404040                       1013+         DC    CL8'VCNF'          instruction name
00001570  00000010                                1014+         DC    A(16)              result length
00001574  0000160C                                1015+         DC    A(RE6)             address of expected resul
00001578  00000000 00000000                       1016+         DS    FD                 gap
00001580  00000000 00000000                       1017+V1O6     DS    XL16               V1 output
00001588  00000000 00000000
00001590  00000000 00000000                       1018+         DS    FD                    gap
00001598  00000000                                1019+FPC_R_6  DS    F                  FPC after instruction
000015A0  00000000 00000000                       1020+         DS    FD                    gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000015A8  40404040 40404040                        1021+          DC    CL8' '            was cross check skipped?
000015B0  00000000 00000000                        1022+          DS    FD                   gap
000015B8  00000000 00000000                        1023+XCO6      DS    XL16              Cross check Output
000015C0  00000000 00000000
000015C8  00000000 00000000                        1024+          DS    FD                   gap
000015D0  00000000                                 1025+FPC_XC_6  DS    F                 FPC after cross check
000015D8  00000000 00000000                        1026+          DS    FD                   gap
000015E0  00000000                                 1027+          DS    F                 debug area
000015E4  00000000                                 1028+          DS    F
                                                   1029+*
000015E8                                           1030+X6        DS    0F
000015E8  B29D 84C4                      000006C4  1031+          LFPC  FPCINIT           initialize FPC
000015EC  E320 500C 0014                 00001564  1032+          LGF   R2,V2_6           get v2
000015F2  E762 0000 0806                 00000000  1033+          VL    V22,0(R2)
000015F8  E666 0001 0C55                           1034+          VCNF  V22,V22,0,1       test instruction (dest is source)
000015FE  B29C 5040                      00001598  1035+          STFPC FPC_R_6           save FPC
00001602  E760 5028 080E                 00001580  1036+          VST   V22,V1O6          save instruction result
00001608  07FB                                     1037+          BR    R11               return
0000160C                                           1038+RE6       DS    0F                expected 16 byte result
0000160C                                           1039+          DROP  R5
0000160C  C5C00000 00000000                        1040           DC    XL16'C5C0000000000000000000000000D800'
00001614  00000000 0000D800
0000161C  CB800000 00000000                        1041           DC    XL16'CB8000000000000000000000000F000'
00001624  00000000 0000F000
                                                   1042
                                                   1043 * 20/7 (about)
                                                   1044           VRR_A VCNF,0,1,00,00,N
00001630                                           1045+          DS    0FD
00001630                         00001630          1046+          USING *,R5              base for test data and test routine
00001630  000016C0                                 1047+T7        DC    A(X7)             address of test routine
00001634  0007                                     1048+          DC    H'7'              test number
00001636  00                                       1049+          DC    X'00'
00001637  D5                                       1050+          DC    CL1'N'            Y = skip cross check
00001638  00                                       1051+          DC    HL1'0'            m3
00001639  01                                       1052+          DC    HL1'1'            m4
0000163A  00                                       1053+FLG7      DC    X'00'             expected FPC flags
0000163B  00                                       1054+VXC7      DC    X'00'             expected VXC
0000163C  000016F4                                 1055+V2_7      DC    A(RE7+16)         address of v2: 16-byte packed decimal
00001640  E5C3D5C6 40404040                        1056+          DC    CL8'VCNF'         instruction name
00001648  00000010                                 1057+          DC    A(16)             result length
0000164C  000016E4                                 1058+          DC    A(RE7)            address of expected resul
00001650  00000000 00000000                        1059+          DS    FD                gap
00001658  00000000 00000000                        1060+V1O7      DS    XL16              V1 output
00001660  00000000 00000000
00001668  00000000 00000000                        1061+          DS    FD                   gap
00001670  00000000                                 1062+FPC_R_7   DS    F                 FPC after instruction
00001678  00000000 00000000                        1063+          DS    FD                   gap
00001680  40404040 40404040                        1064+          DC    CL8' '            was cross check skipped?
00001688  00000000 00000000                        1065+          DS    FD                   gap
00001690  00000000 00000000                        1066+XCO7      DS    XL16              Cross check Output
00001698  00000000 00000000
000016A0  00000000 00000000                        1067+          DS    FD                   gap
000016A8  00000000                                 1068+FPC_XC_7  DS    F                 FPC after cross check
000016B0  00000000 00000000                        1069+          DS    FD                   gap
000016B8  00000000                                 1070+          DS    F                 debug area
000016BC  00000000                                 1071+          DS    F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  1072+*
000016C0                                          1073+X7       DS    0F
000016C0  B29D 84C4                     000006C4  1074+          LFPC  FPCINIT           initialize FPC
000016C4  E320 500C 0014                0000163C  1075+          LGF   R2,V2_7           get v2
000016CA  E762 0000 0806                00000000  1076+          VL    V22,0(R2)
000016D0  E666 0001 0C55                          1077+          VCNF  V22,V22,0,1       test instruction (dest is source)
000016D6  B29C 5040                     00001670  1078+          STFPC FPC_R_7           save FPC
000016DA  E760 5028 080E                00001658  1079+          VST   V22,V1O7          save instruction result
000016E0  07FB                                    1080+          BR    R11               return
000016E4                                          1081+RE7      DS    0F                expected 16 byte result
000016E4                                          1082+          DROP  R5
000016E4  40DB0000 00000000                       1083           DC    XL16'40DB0000000000000000000000D800'
000016EC  00000000 0000D800
000016F4  41B60000 00000000                       1084           DC    XL16'41B60000000000000000000000F000'
000016FC  00000000 0000F000
                                                  1085
                                                  1086 * additional tests
                                                  1087 * max  tiny:  (1 - 2^-11) * 2^16 (65504)
                                                  1088           VRR_A VCNF,0,1,00,00,S                  skip xc - rounded
00001708                                          1089+          DS    0FD
00001708                        00001708          1090+          USING *,R5              base for test data and test routine
00001708  00001798                                1091+T8       DC    A(X8)             address of test routine
0000170C  0008                                    1092+          DC    H'8'              test number
0000170E  00                                      1093+          DC    X'00'
0000170F  E2                                      1094+          DC    CL1'S'            Y = skip cross check
00001710  00                                      1095+          DC    HL1'0'            m3
00001711  01                                      1096+          DC    HL1'1'            m4
00001712  00                                      1097+FLG8     DC    X'00'             expected FPC flags
00001713  00                                      1098+VXC8     DC    X'00'             expected VXC
00001714  000017CC                                1099+V2_8     DC    A(RE8+16)         address of v2: 16-byte packed decimal
00001718  E5C3D5C6 40404040                       1100+          DC    CL8'VCNF'         instruction name
00001720  00000010                                1101+          DC    A(16)             result length
00001724  000017BC                                1102+          DC    A(RE8)            address of expected resul
00001728  00000000 00000000                       1103+          DS    FD                gap
00001730  00000000 00000000                       1104+V1O8     DS    XL16              V1 output
00001738  00000000 00000000
00001740  00000000 00000000                       1105+          DS    FD                   gap
00001748  00000000                                1106+FPC_R_8  DS    F                 FPC after instruction
00001750  00000000 00000000                       1107+          DS    FD                   gap
00001758  40404040 40404040                       1108+          DC    CL8' '            was cross check skipped?
00001760  00000000 00000000                       1109+          DS    FD                   gap
00001768  00000000 00000000                       1110+XCO8     DS    XL16              Cross check Output
00001770  00000000 00000000
00001778  00000000 00000000                       1111+          DS    FD                   gap
00001780  00000000                                1112+FPC_XC_8 DS    F                 FPC after cross check
00001788  00000000 00000000                       1113+          DS    FD                   gap
00001790  00000000                                1114+          DS    F                 debug area
00001794  00000000                                1115+          DS    F
                                                  1116+*
00001798                                          1117+X8       DS    0F
00001798  B29D 84C4                     000006C4  1118+          LFPC  FPCINIT           initialize FPC
0000179C  E320 500C 0014                00001714  1119+          LGF   R2,V2_8           get v2
000017A2  E762 0000 0806                00000000  1120+          VL    V22,0(R2)
000017A8  E666 0001 0C55                          1121+          VCNF  V22,V22,0,1       test instruction (dest is source)
000017AE  B29C 5040                     00001748  1122+          STFPC FPC_R_8           save FPC
000017B2  E760 5028 080E                00001730  1123+          VST   V22,V1O8          save instruction result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000017B8  07FB                                     1124+         BR    R11               return
000017BC                                           1125+RE8      DS    0F                expected 16 byte result
000017BC                                           1126+         DROP  R5
000017BC  5E000000 00000000                        1127          DC    XL16'5E00000000000000000000000000D800'
000017C4  00000000 0000D800
000017CC  7BFF0000 00000000                        1128          DC    XL16'7BFF0000000000000000000000F000'
000017D4  00000000 0000F000
                                                   1129
                                                   1130 * min tiny (normal): 2^-14 (0.00006103515625)
                                                   1131          VRR_A VCNF,0,1,00,00,N
000017E0                                           1132+         DS    0FD
000017E0                      000017E0             1133+         USING *,R5              base for test data and test routine
000017E0  00001870                                 1134+T9       DC    A(X9)             address of test routine
000017E4  0009                                     1135+         DC    H'9'              test number
000017E6  00                                       1136+         DC    X'00'
000017E7  D5                                       1137+         DC    CL1'N'            Y = skip cross check
000017E8  00                                       1138+         DC    HL1'0'            m3
000017E9  01                                       1139+         DC    HL1'1'            m4
000017EA  00                                       1140+FLG9     DC    X'00'             expected FPC flags
000017EB  00                                       1141+VXC9     DC    X'00'             expected VXC
000017EC  000018A4                                 1142+V2_9     DC    A(RE9+16)         address of v2: 16-byte packed decimal
000017F0  E5C3D5C6 40404040                        1143+         DC    CL8'VCNF'         instruction name
000017F8  00000010                                 1144+         DC    A(16)             result length
000017FC  00001894                                 1145+         DC    A(RE9)            address of expected resul
00001800  00000000 00000000                        1146+         DS    FD                gap
00001808  00000000 00000000                        1147+V1O9     DS    XL16              V1 output
00001810  00000000 00000000
00001818  00000000 00000000                        1148+         DS    FD                   gap
00001820  00000000                                 1149+FPC_R_9  DS    F                 FPC after instruction
00001828  00000000 00000000                        1150+         DS    FD                   gap
00001830  40404040 40404040                        1151+         DC    CL8' '            was cross check skipped?
00001838  00000000 00000000                        1152+         DS    FD                   gap
00001840  00000000 00000000                        1153+XCO9     DS    XL16              Cross check Output
00001848  00000000 00000000
00001850  00000000 00000000                        1154+         DS    FD                   gap
00001858  00000000                                 1155+FPC_XC_9 DS    F                 FPC after cross check
00001860  00000000 00000000                        1156+         DS    FD                   gap
00001868  00000000                                 1157+         DS    F                 debug area
0000186C  00000000                                 1158+         DS    F
                                                   1159+*
00001870                                           1160+X9       DS    0F
00001870  B29D 84C4                   000006C4     1161+         LFPC  FPCINIT           initialize FPC
00001874  E320 500C 0014              000017EC     1162+         LGF   R2,V2_9           get v2
0000187A  E762 0000 0806              00000000     1163+         VL    V22,0(R2)
00001880  E666 0001 0C55                           1164+         VCNF  V22,V22,0,1       test instruction (dest is source)
00001886  B29C 5040                   00001820     1165+         STFPC FPC_R_9           save FPC
0000188A  E760 5028 080E              00001808     1166+         VST   V22,V1O9          save instruction result
00001890  07FB                                     1167+         BR    R11               return
00001894                                           1168+RE9      DS    0F                expected 16 byte result
00001894                                           1169+         DROP  R5
00001894  22000000 00000000                        1170          DC    XL16'22000000000000000000000000D800'
0000189C  00000000 0000D800
000018A4  04000000 00000000                        1171          DC    XL16'04000000000000000000000000F000'
000018AC  00000000 0000F000
                                                   1172
                                                   1173 * min tiny (subnormal): 2^-24 (0.00000059604644775390625)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    1174          VRR_A VCNF,0,1,00,00,N
000018B8                                            1175+         DS    0FD
000018B8                              000018B8      1176+         USING *,R5              base for test data and test routine
000018B8  00001948                                  1177+T10      DC    A(X10)            address of test routine
000018BC  000A                                      1178+         DC    H'10'             test number
000018BE  00                                        1179+         DC    X'00'
000018BF  D5                                        1180+         DC    CL1'N'            Y = skip cross check
000018C0  00                                        1181+         DC    HL1'0'            m3
000018C1  01                                        1182+         DC    HL1'1'            m4
000018C2  00                                        1183+FLG10    DC    X'00'             expected FPC flags
000018C3  00                                        1184+VXC10    DC    X'00'             expected VXC
000018C4  0000197C                                  1185+V2_10    DC    A(RE10+16)        address of v2: 16-byte packed decimal
000018C8  E5C3D5C6 40404040                         1186+         DC    CL8'VCNF'         instruction name
000018D0  00000010                                  1187+         DC    A(16)             result length
000018D4  0000196C                                  1188+         DC    A(RE10)           address of expected resul
000018D8  00000000 00000000                         1189+         DS    FD                gap
000018E0  00000000 00000000                         1190+V1O10    DS    XL16              V1 output
000018E8  00000000 00000000
000018F0  00000000 00000000                         1191+         DS    FD                   gap
000018F8  00000000                                  1192+FPC_R_10 DS    F                 FPC after instruction
00001900  00000000 00000000                         1193+         DS    FD                   gap
00001908  40404040 40404040                         1194+         DC    CL8' '            was cross check skipped?
00001910  00000000 00000000                         1195+         DS    FD                   gap
00001918  00000000 00000000                         1196+XCO10    DS    XL16              Cross check Output
00001920  00000000 00000000
00001928  00000000 00000000                         1197+         DS    FD                   gap
00001930  00000000                                  1198+FPC_XC_10 DS   F                 FPC after cross check
00001938  00000000 00000000                         1199+         DS    FD                   gap
00001940  00000000                                  1200+         DS    F                 debug area
00001944  00000000                                  1201+         DS    F
                                                    1202+*
00001948                                            1203+X10      DS    0F
00001948  B29D 84C4                       000006C4  1204+         LFPC  FPCINIT           initialize FPC
0000194C  E320 500C 0014                  000018C4  1205+         LGF   R2,V2_10          get v2
00001952  E762 0000 0806                  00000000  1206+         VL    V22,0(R2)
00001958  E666 0001 0C55                            1207+         VCNF  V22,V22,0,1       test instruction (dest is source)
0000195E  B29C 5040                       000018F8  1208+         STFPC FPC_R_10          save FPC
00001962  E760 5028 080E                  000018E0  1209+         VST   V22,V1O10         save instruction result
00001968  07FB                                      1210+         BR    R11               return
0000196C                                            1211+RE10     DS    0F                expected 16 byte result
0000196C                                            1212+         DROP  R5
0000196C  0E000000 00000000                         1213          DC    XL16'0E000000000000000000000000D800'
00001974  00000000 0000D800
0000197C  00010000 00000000                         1214          DC    XL16'00010000000000000000000000F000'
00001984  00000000 0000F000
                                                    1215
                                                    1216 * NAN,
                                                    1217          VRR_A VCNF,0,1,00,00,S           skip xcheck - includes NAN
00001990                                            1218+         DS    0FD
00001990                              00001990      1219+         USING *,R5              base for test data and test routine
00001990  00001A20                                  1220+T11      DC    A(X11)            address of test routine
00001994  000B                                      1221+         DC    H'11'             test number
00001996  00                                        1222+         DC    X'00'
00001997  E2                                        1223+         DC    CL1'S'            Y = skip cross check
00001998  00                                        1224+         DC    HL1'0'            m3
00001999  01                                        1225+         DC    HL1'1'            m4
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000199A  00                                       1226+FLG11    DC    X'00'             expected FPC flags
0000199B  00                                       1227+VXC11    DC    X'00'             expected VXC
0000199C  00001A54                                 1228+V2_11    DC    A(RE11+16)        address of v2: 16-byte packed decimal
000019A0  E5C3D5C6 40404040                        1229+         DC    CL8'VCNF'         instruction name
000019A8  00000010                                 1230+         DC    A(16)             result length
000019AC  00001A44                                 1231+         DC    A(RE11)           address of expected resul
000019B0  00000000 00000000                        1232+         DS    FD                gap
000019B8  00000000 00000000                        1233+V1O11    DS    XL16              V1 output
000019C0  00000000 00000000
000019C8  00000000 00000000                        1234+         DS    FD                   gap
000019D0  00000000                                 1235+FPC_R_11 DS    F                 FPC after instruction
000019D8  00000000 00000000                        1236+         DS    FD                   gap
000019E0  40404040 40404040                        1237+         DC    CL8' '            was cross check skipped?
000019E8  00000000 00000000                        1238+         DS    FD                   gap
000019F0  00000000 00000000                        1239+XCO11    DS    XL16              Cross check Output
000019F8  00000000 00000000
00001A00  00000000 00000000                        1240+         DS    FD                   gap
00001A08  00000000                                 1241+FPC_XC_11 DS   F                 FPC after cross check
00001A10  00000000 00000000                        1242+         DS    FD                   gap
00001A18  00000000                                 1243+         DS    F                 debug area
00001A1C  00000000                                 1244+         DS    F
                                                   1245+*
00001A20                                           1246+X11      DS    0F
00001A20  B29D 84C4                     000006C4   1247+         LFPC  FPCINIT           initialize FPC
00001A24  E320 500C 0014                0000199C   1248+         LGF   R2,V2_11          get v2
00001A2A  E762 0000 0806                00000000   1249+         VL    V22,0(R2)
00001A30  E666 0001 0C55                           1250+         VCNF  V22,V22,0,1       test instruction (dest is source)
00001A36  B29C 5040                     000019D0   1251+         STFPC FPC_R_11          save FPC
00001A3A  E760 5028 080E                000019B8   1252+         VST   V22,V1O11         save instruction result
00001A40  07FB                                     1253+         BR    R11               return
00001A44                                           1254+RE11     DS    0F                expected 16 byte result
00001A44                                           1255+         DROP  R5
00001A44  FFFF0000 00000000                        1256          DC    XL16'FFFF0000000000000000000000D800'
00001A4C  00000000 0000D800
00001A54  FFFF0000 00000000                        1257          DC    XL16'FFFF0000000000000000000000F000'
00001A5C  00000000 0000F000
                                                   1258
                                                   1259 * inexact - bad m3, m4
                                                   1260          VRR_A VCNF,1,0,08,05,S                    skip xc - inexact
00001A68                                           1261+         DS    0FD
00001A68                        00001A68           1262+         USING *,R5              base for test data and test routine
00001A68  00001AF8                                 1263+T12      DC    A(X12)            address of test routine
00001A6C  000C                                     1264+         DC    H'12'             test number
00001A6E  00                                       1265+         DC    X'00'
00001A6F  E2                                       1266+         DC    CL1'S'            Y = skip cross check
00001A70  01                                       1267+         DC    HL1'1'            m3
00001A71  00                                       1268+         DC    HL1'0'            m4
00001A72  08                                       1269+FLG12    DC    X'08'             expected FPC flags
00001A73  05                                       1270+VXC12    DC    X'05'             expected VXC
00001A74  00001B2C                                 1271+V2_12    DC    A(RE12+16)        address of v2: 16-byte packed decimal
00001A78  E5C3D5C6 40404040                        1272+         DC    CL8'VCNF'         instruction name
00001A80  00000010                                 1273+         DC    A(16)             result length
00001A84  00001B1C                                 1274+         DC    A(RE12)           address of expected resul
00001A88  00000000 00000000                        1275+         DS    FD                gap
00001A90  00000000 00000000                        1276+V1O12    DS    XL16              V1 output
00001A98  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001AA0  00000000 00000000                      1277+          DS    FD                  gap
00001AA8  00000000                               1278+FPC_R_12  DS    F                   FPC after instruction
00001AB0  00000000 00000000                      1279+          DS    FD                  gap
00001AB8  40404040 40404040                      1280+          DC    CL8' '              was cross check skipped?
00001AC0  00000000 00000000                      1281+          DS    FD                  gap
00001AC8  00000000 00000000                      1282+XCO12     DS    XL16                Cross check Output
00001AD0  00000000 00000000
00001AD8  00000000 00000000                      1283+          DS    FD                  gap
00001AE0  00000000                               1284+FPC_XC_12 DS    F                   FPC after cross check
00001AE8  00000000 00000000                      1285+          DS    FD                  gap
00001AF0  00000000                               1286+          DS    F                   debug area
00001AF4  00000000                               1287+          DS    F
                                                 1288+*
00001AF8                                         1289+X12       DS    0F
00001AF8  B29D 84C4                   000006C4   1290+          LFPC  FPCINIT             initialize FPC
00001AFC  E320 500C 0014              00001A74   1291+          LGF   R2,V2_12            get v2
00001B02  E762 0000 0806              00000000   1292+          VL    V22,0(R2)
00001B08  E666 0000 1C55                         1293+          VCNF  V22,V22,1,0         test instruction (dest is source)
00001B0E  B29C 5040                   00001AA8   1294+          STFPC FPC_R_12            save FPC
00001B12  E760 5028 080E              00001A90   1295+          VST   V22,V1O12           save instruction result
00001B18  07FB                                   1296+          BR    R11                 return
00001B1C                                         1297+RE12      DS    0F                  expected 16 byte result
00001B1C                                         1298+          DROP  R5
00001B1C  00000000 00000000                      1299           DC    XL16'00000000000000000000000000000000'    not checked
00001B24  00000000 00000000
00001B2C  00010000 00000000                      1300           DC    XL16'00010000000000000000000000000F000'
00001B34  00000000 0000F000
                                                 1301
                                                 1302 *-------------------------------------------------------------------
                                                 1303 * VCLFNH   - VECTOR FP CONVERT AND LENGTHEN FROM NNP HIGH
                                                 1304 *-------------------------------------------------------------------
                                                 1305 *  dlfloat -> short float (with cross check: short float -> dlfloat)
                                                 1306 *
                                                 1307
                                                 1308 * +0, -0     simple instruction and 'test' test
                                                 1309           VRR_A VCLFNH,2,0,00,00,N
00001B40                                         1310+          DS    0FD
00001B40                        00001B40         1311+          USING *,R5                base for test data and test routine
00001B40  00001BD0                               1312+T13       DC    A(X13)              address of test routine
00001B44  000D                                   1313+          DC    H'13'               test number
00001B46  00                                     1314+          DC    X'00'
00001B47  D5                                     1315+          DC    CL1'N'              Y = skip cross check
00001B48  02                                     1316+          DC    HL1'2'              m3
00001B49  00                                     1317+          DC    HL1'0'              m4
00001B4A  00                                     1318+FLG13     DC    X'00'               expected FPC flags
00001B4B  00                                     1319+VXC13     DC    X'00'               expected VXC
00001B4C  00001C04                               1320+V2_13     DC    A(RE13+16)          address of v2: 16-byte packed decimal
00001B50  E5C3D3C6 D5C84040                      1321+          DC    CL8'VCLFNH'         instruction name
00001B58  00000010                               1322+          DC    A(16)               result length
00001B5C  00001BF4                               1323+          DC    A(RE13)             address of expected resul
00001B60  00000000 00000000                      1324+          DS    FD                  gap
00001B68  00000000 00000000                      1325+V1O13     DS    XL16                V1 output
00001B70  00000000 00000000
00001B78  00000000 00000000                      1326+          DS    FD                  gap
00001B80  00000000                               1327+FPC_R_13  DS    F                   FPC after instruction
00001B88  00000000 00000000                      1328+          DS    FD                  gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001B90  40404040 40404040                        1329+          DC    CL8' '            was cross check skipped?
00001B98  00000000 00000000                        1330+          DS    FD                   gap
00001BA0  00000000 00000000                        1331+XCO13     DS    XL16              Cross check Output
00001BA8  00000000 00000000
00001BB0  00000000 00000000                        1332+          DS    FD                   gap
00001BB8  00000000                                 1333+FPC_XC_13 DS    F                 FPC after cross check
00001BC0  00000000 00000000                        1334+          DS    FD                   gap
00001BC8  00000000                                 1335+          DS    F                 debug area
00001BCC  00000000                                 1336+          DS    F
                                                   1337+*
00001BD0                                           1338+X13       DS    0F
00001BD0  B29D 84C4                       000006C4 1339+          LFPC  FPCINIT           initialize FPC
00001BD4  E320 500C 0014                  00001B4C 1340+          LGF   R2,V2_13          get v2
00001BDA  E762 0000 0806                  00000000 1341+          VL    V22,0(R2)
00001BE0  E666 0000 2C56                           1342+          VCLFNH V22,V22,2,0      test instruction (dest is source)
00001BE6  B29C 5040                       00001B80 1343+          STFPC FPC_R_13          save FPC
00001BEA  E760 5028 080E                  00001B68 1344+          VST   V22,V1O13         save instruction result
00001BF0  07FB                                     1345+          BR    R11               return
00001BF4                                           1346+RE13      DS    0F                expected 16 byte result
00001BF4                                           1347+          DROP  R5
00001BF4  00000000 80000000                        1348           DC    XL16'00000000800000000000000000000000'
00001BFC  00000000 00000000
00001C04  00008000 00000000                        1349           DC    XL16'00008000000000000000000000000000'
00001C0C  00000000 00000000
                                                   1350
                                                   1351 * +1, -1
                                                   1352           VRR_A VCLFNH,2,0,00,00,N
00001C18                                           1353+          DS    0FD
00001C18                        00001C18           1354+          USING *,R5              base for test data and test routine
00001C18  00001CA8                                 1355+T14       DC    A(X14)            address of test routine
00001C1C  000E                                     1356+          DC    H'14'             test number
00001C1E  00                                       1357+          DC    X'00'
00001C1F  D5                                       1358+          DC    CL1'N'            Y = skip cross check
00001C20  02                                       1359+          DC    HL1'2'            m3
00001C21  00                                       1360+          DC    HL1'0'            m4
00001C22  00                                       1361+FLG14     DC    X'00'             expected FPC flags
00001C23  00                                       1362+VXC14     DC    X'00'             expected VXC
00001C24  00001CDC                                 1363+V2_14     DC    A(RE14+16)        address of v2: 16-byte packed decimal
00001C28  E5C3D3C6 D5C84040                        1364+          DC    CL8'VCLFNH'       instruction name
00001C30  00000010                                 1365+          DC    A(16)             result length
00001C34  00001CCC                                 1366+          DC    A(RE14)           address of expected resul
00001C38  00000000 00000000                        1367+          DS    FD                gap
00001C40  00000000 00000000                        1368+V1O14     DS    XL16              V1 output
00001C48  00000000 00000000
00001C50  00000000 00000000                        1369+          DS    FD                   gap
00001C58  00000000                                 1370+FPC_R_14  DS    F                 FPC after instruction
00001C60  00000000 00000000                        1371+          DS    FD                   gap
00001C68  40404040 40404040                        1372+          DC    CL8' '            was cross check skipped?
00001C70  00000000 00000000                        1373+          DS    FD                   gap
00001C78  00000000 00000000                        1374+XCO14     DS    XL16              Cross check Output
00001C80  00000000 00000000
00001C88  00000000 00000000                        1375+          DS    FD                   gap
00001C90  00000000                                 1376+FPC_XC_14 DS    F                 FPC after cross check
00001C98  00000000 00000000                        1377+          DS    FD                   gap
00001CA0  00000000                                 1378+          DS    F                 debug area
00001CA4  00000000                                 1379+          DS    F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  1380+*
00001CA8                                          1381+X14      DS    0F
00001CA8  B29D 84C4                     000006C4  1382+          LFPC  FPCINIT           initialize FPC
00001CAC  E320 500C 0014                00001C24  1383+          LGF   R2,V2_14          get v2
00001CB2  E762 0000 0806                00000000  1384+          VL    V22,0(R2)
00001CB8  E666 0000 2C56                          1385+          VCLFNH V22,V22,2,0      test instruction (dest is source)
00001CBE  B29C 5040                     00001C58  1386+          STFPC FPC_R_14          save FPC
00001CC2  E760 5028 080E                00001C40  1387+          VST   V22,V1O14         save instruction result
00001CC8  07FB                                    1388+          BR    R11               return
00001CCC                                          1389+RE14      DS    0F                expected 16 byte result
00001CCC                                          1390+          DROP  R5
00001CCC  3F800000 BF800000                       1391           DC    XL16'3F800000BF800000000000000000000000'
00001CD4  00000000 00000000
00001CDC  3E00BE00 00000000                       1392           DC    XL16'3E00BE000000000000000000000000000'
00001CE4  00000000 00000000
                                                  1393
                                                  1394 * +0.5, -0.5
                                                  1395           VRR_A VCLFNH,2,0,00,00,N
00001CF0                                          1396+          DS    0FD
00001CF0                        00001CF0          1397+          USING *,R5              base for test data and test routine
00001CF0  00001D80                                1398+T15       DC    A(X15)            address of test routine
00001CF4  000F                                    1399+          DC    H'15'             test number
00001CF6  00                                      1400+          DC    X'00'
00001CF7  D5                                      1401+          DC    CL1'N'            Y = skip cross check
00001CF8  02                                      1402+          DC    HL1'2'            m3
00001CF9  00                                      1403+          DC    HL1'0'            m4
00001CFA  00                                      1404+FLG15     DC    X'00'             expected FPC flags
00001CFB  00                                      1405+VXC15     DC    X'00'             expected VXC
00001CFC  00001DB4                                1406+V2_15     DC    A(RE15+16)        address of v2: 16-byte packed decimal
00001D00  E5C3D3C6 D5C84040                       1407+          DC    CL8'VCLFNH'       instruction name
00001D08  00000010                                1408+          DC    A(16)             result length
00001D0C  00001DA4                                1409+          DC    A(RE15)           address of expected resul
00001D10  00000000 00000000                       1410+          DS    FD                gap
00001D18  00000000 00000000                       1411+V1O15     DS    XL16              V1 output
00001D20  00000000 00000000
00001D28  00000000 00000000                       1412+          DS    FD                   gap
00001D30  00000000                                1413+FPC_R_15  DS    F                 FPC after instruction
00001D38  00000000 00000000                       1414+          DS    FD                   gap
00001D40  40404040 40404040                       1415+          DC    CL8' '            was cross check skipped?
00001D48  00000000 00000000                       1416+          DS    FD                   gap
00001D50  00000000 00000000                       1417+XCO15     DS    XL16              Cross check Output
00001D58  00000000 00000000
00001D60  00000000 00000000                       1418+          DS    FD                   gap
00001D68  00000000                                1419+FPC_XC_15 DS    F                 FPC after cross check
00001D70  00000000 00000000                       1420+          DS    FD                   gap
00001D78  00000000                                1421+          DS    F                 debug area
00001D7C  00000000                                1422+          DS    F
                                                  1423+*
00001D80                                          1424+X15       DS    0F
00001D80  B29D 84C4                     000006C4  1425+          LFPC  FPCINIT           initialize FPC
00001D84  E320 500C 0014                00001CFC  1426+          LGF   R2,V2_15          get v2
00001D8A  E762 0000 0806                00000000  1427+          VL    V22,0(R2)
00001D90  E666 0000 2C56                          1428+          VCLFNH V22,V22,2,0      test instruction (dest is source)
00001D96  B29C 5040                     00001D30  1429+          STFPC FPC_R_15          save FPC
00001D9A  E760 5028 080E                00001D18  1430+          VST   V22,V1O15         save instruction result
00001DA0  07FB                                    1431+          BR    R11               return
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001DA4                                           1432+RE15     DS    0F                expected 16 byte result
00001DA4                                           1433+         DROP  R5
00001DA4  3F000000 BF000000                        1434          DC    XL16'3F000000BF000000000000000000000000'
00001DAC  00000000 00000000
00001DB4  3C00BC00 00000000                        1435          DC    XL16'3C00BC000000000000000000000000'
00001DBC  00000000 00000000
                                                   1436
                                                   1437 * 1/64, -1/64
                                                   1438          VRR_A VCLFNH,2,0,00,00,N
00001DC8                                           1439+         DS    0FD
00001DC8                          00001DC8         1440+         USING *,R5              base for test data and test routine
00001DC8  00001E58                                 1441+T16      DC    A(X16)            address of test routine
00001DCC  0010                                     1442+         DC    H'16'             test number
00001DCE  00                                       1443+         DC    X'00'
00001DCF  D5                                       1444+         DC    CL1'N'            Y = skip cross check
00001DD0  02                                       1445+         DC    HL1'2'            m3
00001DD1  00                                       1446+         DC    HL1'0'            m4
00001DD2  00                                       1447+FLG16    DC    X'00'             expected FPC flags
00001DD3  00                                       1448+VXC16    DC    X'00'             expected VXC
00001DD4  00001E8C                                 1449+V2_16    DC    A(RE16+16)        address of v2: 16-byte packed decimal
00001DD8  E5C3D3C6 D5C84040                        1450+         DC    CL8'VCLFNH'       instruction name
00001DE0  00000010                                 1451+         DC    A(16)             result length
00001DE4  00001E7C                                 1452+         DC    A(RE16)           address of expected resul
00001DE8  00000000 00000000                        1453+         DS    FD                gap
00001DF0  00000000 00000000                        1454+V1O16    DS    XL16              V1 output
00001DF8  00000000 00000000
00001E00  00000000 00000000                        1455+         DS    FD                   gap
00001E08  00000000                                 1456+FPC_R_16 DS    F                 FPC after instruction
00001E10  00000000 00000000                        1457+         DS    FD                   gap
00001E18  40404040 40404040                        1458+         DC    CL8' '            was cross check skipped?
00001E20  00000000 00000000                        1459+         DS    FD                   gap
00001E28  00000000 00000000                        1460+XCO16    DS    XL16              Cross check Output
00001E30  00000000 00000000
00001E38  00000000 00000000                        1461+         DS    FD                   gap
00001E40  00000000                                 1462+FPC_XC_16 DS   F                 FPC after cross check
00001E48  00000000 00000000                        1463+         DS    FD                   gap
00001E50  00000000                                 1464+         DS    F                 debug area
00001E54  00000000                                 1465+         DS    F
                                                   1466+*
00001E58                                           1467+X16      DS    0F
00001E58  B29D 84C4                      000006C4  1468+         LFPC  FPCINIT           initialize FPC
00001E5C  E320 500C 0014                 00001DD4  1469+         LGF   R2,V2_16          get v2
00001E62  E762 0000 0806                 00000000  1470+         VL    V22,0(R2)
00001E68  E666 0000 2C56                           1471+         VCLFNH V22,V22,2,0      test instruction (dest is source)
00001E6E  B29C 5040                      00001E08  1472+         STFPC FPC_R_16          save FPC
00001E72  E760 5028 080E                 00001DF0  1473+         VST   V22,V1O16         save instruction result
00001E78  07FB                                     1474+         BR    R11               return
00001E7C                                           1475+RE16     DS    0F                expected 16 byte result
00001E7C                                           1476+         DROP  R5
00001E7C  3C800000 BC800000                        1477          DC    XL16'3C800000BC800000000000000000000000'
00001E84  00000000 00000000
00001E8C  3200B200 00000000                        1478          DC    XL16'3200B200000000000000000000000000'
00001E94  00000000 00000000
                                                   1479
                                                   1480 * +15, -15
                                                   1481          VRR_A VCLFNH,2,0,00,00,N
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001EA0                                          1482+          DS    0FD
00001EA0                       00001EA0           1483+          USING *,R5              base for test data and test routine
00001EA0  00001F30                                1484+T17       DC    A(X17)            address of test routine
00001EA4  0011                                    1485+          DC    H'17'             test number
00001EA6  00                                      1486+          DC    X'00'
00001EA7  D5                                      1487+          DC    CL1'N'            Y = skip cross check
00001EA8  02                                      1488+          DC    HL1'2'            m3
00001EA9  00                                      1489+          DC    HL1'0'            m4
00001EAA  00                                      1490+FLG17     DC    X'00'             expected FPC flags
00001EAB  00                                      1491+VXC17     DC    X'00'             expected VXC
00001EAC  00001F64                                1492+V2_17     DC    A(RE17+16)        address of v2: 16-byte packed decimal
00001EB0  E5C3D3C6 D5C84040                       1493+          DC    CL8'VCLFNH'       instruction name
00001EB8  00000010                                1494+          DC    A(16)             result length
00001EBC  00001F54                                1495+          DC    A(RE17)           address of expected resul
00001EC0  00000000 00000000                       1496+          DS    FD                gap
00001EC8  00000000 00000000                       1497+V1O17     DS    XL16              V1 output
00001ED0  00000000 00000000
00001ED8  00000000 00000000                       1498+          DS    FD                   gap
00001EE0  00000000                                1499+FPC_R_17  DS    F                 FPC after instruction
00001EE8  00000000 00000000                       1500+          DS    FD                   gap
00001EF0  40404040 40404040                       1501+          DC    CL8' '            was cross check skipped?
00001EF8  00000000 00000000                       1502+          DS    FD                   gap
00001F00  00000000 00000000                       1503+XCO17     DS    XL16              Cross check Output
00001F08  00000000 00000000
00001F10  00000000 00000000                       1504+          DS    FD                   gap
00001F18  00000000                                1505+FPC_XC_17 DS    F                 FPC after cross check
00001F20  00000000 00000000                       1506+          DS    FD                   gap
00001F28  00000000                                1507+          DS    F                 debug area
00001F2C  00000000                                1508+          DS    F
                                                  1509+*
00001F30                                          1510+X17       DS    0F
00001F30  B29D 84C4                    000006C4   1511+          LFPC  FPCINIT           initialize FPC
00001F34  E320 500C 0014               00001EAC   1512+          LGF   R2,V2_17          get v2
00001F3A  E762 0000 0806               00000000   1513+          VL    V22,0(R2)
00001F40  E666 0000 2C56                          1514+          VCLFNH V22,V22,2,0      test instruction (dest is source)
00001F46  B29C 5040                    00001EE0   1515+          STFPC FPC_R_17          save FPC
00001F4A  E760 5028 080E               00001EC8   1516+          VST   V22,V1O17         save instruction result
00001F50  07FB                                    1517+          BR    R11               return
00001F54                                          1518+RE17      DS    0F                expected 16 byte result
00001F54                                          1519+          DROP  R5
00001F54  41700000 C1700000                       1520           DC    XL16'41700000C1700000000000000000000'
00001F5C  00000000 00000000
00001F64  45C0C5C0 00000000                       1521           DC    XL16'45C0C5C00000000000000000000000'
00001F6C  00000000 00000000
                                                  1522
                                                  1523 * +20/7, -20/7 (about)
                                                  1524           VRR_A VCLFNH,2,0,00,00,N
00001F78                                          1525+          DS    0FD
00001F78                       00001F78           1526+          USING *,R5              base for test data and test routine
00001F78  00002008                                1527+T18       DC    A(X18)            address of test routine
00001F7C  0012                                    1528+          DC    H'18'             test number
00001F7E  00                                      1529+          DC    X'00'
00001F7F  D5                                      1530+          DC    CL1'N'            Y = skip cross check
00001F80  02                                      1531+          DC    HL1'2'            m3
00001F81  00                                      1532+          DC    HL1'0'            m4
00001F82  00                                      1533+FLG18     DC    X'00'             expected FPC flags
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001F83  00                                     1534+VXC18    DC    X'00'             expected VXC
00001F84  0000203C                               1535+V2_18    DC    A(RE18+16)        address of v2: 16-byte packed decimal
00001F88  E5C3D3C6 D5C84040                      1536+         DC    CL8'VCLFNH'       instruction name
00001F90  00000010                               1537+         DC    A(16)             result length
00001F94  0000202C                               1538+         DC    A(RE18)           address of expected resul
00001F98  00000000 00000000                      1539+         DS    FD                gap
00001FA0  00000000 00000000                      1540+V1O18    DS    XL16              V1 output
00001FA8  00000000 00000000
00001FB0  00000000 00000000                      1541+         DS    FD                   gap
00001FB8  00000000                               1542+FPC_R_18 DS    F                 FPC after instruction
00001FC0  00000000 00000000                      1543+         DS    FD                   gap
00001FC8  40404040 40404040                      1544+         DC    CL8' '            was cross check skipped?
00001FD0  00000000 00000000                      1545+         DS    FD                   gap
00001FD8  00000000 00000000                      1546+XCO18    DS    XL16              Cross check Output
00001FE0  00000000 00000000
00001FE8  00000000 00000000                      1547+         DS    FD                   gap
00001FF0  00000000                               1548+FPC_XC_18 DS   F                 FPC after cross check
00001FF8  00000000 00000000                      1549+         DS    FD                   gap
00002000  00000000                               1550+         DS    F                 debug area
00002004  00000000                               1551+         DS    F
                                                 1552+*
00002008                                         1553+X18      DS    0F
00002008  B29D 84C4                   000006C4   1554+         LFPC  FPCINIT           initialize FPC
0000200C  E320 500C 0014              00001F84   1555+         LGF   R2,V2_18          get v2
00002012  E762 0000 0806              00000000   1556+         VL    V22,0(R2)
00002018  E666 0000 2C56                         1557+         VCLFNH V22,V22,2,0      test instruction (dest is source)
0000201E  B29C 5040                   00001FB8   1558+         STFPC FPC_R_18          save FPC
00002022  E760 5028 080E              00001FA0   1559+         VST   V22,V1O18         save instruction result
00002028  07FB                                   1560+         BR    R11               return
0000202C                                         1561+RE18     DS    0F                expected 16 byte result
0000202C                                         1562+         DROP  R5
0000202C  4036C000 C036C000                      1563          DC    XL16'4036C000C036C000000000000000000'
00002034  00000000 00000000
0000203C  40DBC0DB 00000000                      1564          DC    XL16'40DBC0DB00000000000000000000000'
00002044  00000000 00000000
                                                 1565
                                                 1566 * additional tests
                                                 1567 * max  tiny:  (1 - 2^-11) * 2^16 (65504)
                                                 1568          VRR_A VCLFNH,2,0,00,00,N
00002050                                         1569+         DS    0FD
00002050                        00002050         1570+         USING *,R5              base for test data and test routine
00002050  000020E0                               1571+T19      DC    A(X19)            address of test routine
00002054  0013                                   1572+         DC    H'19'             test number
00002056  00                                     1573+         DC    X'00'
00002057  D5                                     1574+         DC    CL1'N'            Y = skip cross check
00002058  02                                     1575+         DC    HL1'2'            m3
00002059  00                                     1576+         DC    HL1'0'            m4
0000205A  00                                     1577+FLG19    DC    X'00'             expected FPC flags
0000205B  00                                     1578+VXC19    DC    X'00'             expected VXC
0000205C  00002114                               1579+V2_19    DC    A(RE19+16)        address of v2: 16-byte packed decimal
00002060  E5C3D3C6 D5C84040                      1580+         DC    CL8'VCLFNH'       instruction name
00002068  00000010                               1581+         DC    A(16)             result length
0000206C  00002104                               1582+         DC    A(RE19)           address of expected resul
00002070  00000000 00000000                      1583+         DS    FD                gap
00002078  00000000 00000000                      1584+V1O19    DS    XL16              V1 output
00002080  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002088  00000000 00000000                       1585+          DS    FD                   gap
00002090  00000000                                1586+FPC_R_19  DS    F                  FPC after instruction
00002098  00000000 00000000                       1587+          DS    FD                   gap
000020A0  40404040 40404040                       1588+          DC    CL8' '             was cross check skipped?
000020A8  00000000 00000000                       1589+          DS    FD                   gap
000020B0  00000000 00000000                       1590+XCO19     DS    XL16               Cross check Output
000020B8  00000000 00000000
000020C0  00000000 00000000                       1591+          DS    FD                   gap
000020C8  00000000                                1592+FPC_XC_19 DS    F                  FPC after cross check
000020D0  00000000 00000000                       1593+          DS    FD                   gap
000020D8  00000000                                1594+          DS    F                  debug area
000020DC  00000000                                1595+          DS    F
                                                  1596+*
000020E0                                          1597+X19       DS    0F
000020E0  B29D 84C4                     000006C4  1598+          LFPC  FPCINIT            initialize FPC
000020E4  E320 500C 0014                0000205C  1599+          LGF   R2,V2_19           get v2
000020EA  E762 0000 0806                00000000  1600+          VL    V22,0(R2)
000020F0  E666 0000 2C56                          1601+          VCLFNH V22,V22,2,0       test instruction (dest is source)
000020F6  B29C 5040                     00002090  1602+          STFPC FPC_R_19           save FPC
000020FA  E760 5028 080E                00002078  1603+          VST   V22,V1O19          save instruction result
00002100  07FB                                    1604+          BR    R11                return
00002104                                          1605+RE19      DS    0F                 expected 16 byte result
00002104                                          1606+          DROP  R5
00002104  47800000 00000000                       1607           DC    XL16'47800000000000000000000000000000'
0000210C  00000000 00000000
00002114  5E000000 00000000                       1608           DC    XL16'5E00000000000000000000000000000000'
0000211C  00000000 00000000
                                                  1609
                                                  1610 * max  dlfloat:  2^(33)-2ulp
                                                  1611             VRR_A VCLFNH,2,0,00,00,N
00002128                                          1612+          DS    0FD
00002128                        00002128          1613+          USING *,R5               base for test data and test routine
00002128  000021B8                                1614+T20       DC    A(X20)             address of test routine
0000212C  0014                                    1615+          DC    H'20'              test number
0000212E  00                                      1616+          DC    X'00'
0000212F  D5                                      1617+          DC    CL1'N'             Y = skip cross check
00002130  02                                      1618+          DC    HL1'2'             m3
00002131  00                                      1619+          DC    HL1'0'             m4
00002132  00                                      1620+FLG20     DC    X'00'              expected FPC flags
00002133  00                                      1621+VXC20     DC    X'00'              expected VXC
00002134  000021EC                                1622+V2_20     DC    A(RE20+16)         address of v2: 16-byte packed decimal
00002138  E5C3D3C6 D5C84040                       1623+          DC    CL8'VCLFNH'        instruction name
00002140  00000010                                1624+          DC    A(16)              result length
00002144  000021DC                                1625+          DC    A(RE20)            address of expected resul
00002148  00000000 00000000                       1626+          DS    FD                 gap
00002150  00000000 00000000                       1627+V1O20     DS    XL16               V1 output
00002158  00000000 00000000
00002160  00000000 00000000                       1628+          DS    FD                   gap
00002168  00000000                                1629+FPC_R_20  DS    F                  FPC after instruction
00002170  00000000 00000000                       1630+          DS    FD                   gap
00002178  40404040 40404040                       1631+          DC    CL8' '             was cross check skipped?
00002180  00000000 00000000                       1632+          DS    FD                   gap
00002188  00000000 00000000                       1633+XCO20     DS    XL16               Cross check Output
00002190  00000000 00000000
00002198  00000000 00000000                       1634+          DS    FD                   gap
000021A0  00000000                                1635+FPC_XC_20 DS    F                  FPC after cross check
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000021A8  00000000 00000000                       1636+          DS    FD                   gap
000021B0  00000000                                1637+          DS    F                  debug area
000021B4  00000000                                1638+          DS    F
                                                  1639+*
000021B8                                          1640+X20       DS    0F
000021B8  B29D 84C4                     000006C4  1641+          LFPC  FPCINIT            initialize FPC
000021BC  E320 500C 0014                00002134  1642+          LGF   R2,V2_20           get v2
000021C2  E762 0000 0806                00000000  1643+          VL    V22,0(R2)
000021C8  E666 0000 2C56                          1644+          VCLFNH V22,V22,2,0       test instruction (dest is source)
000021CE  B29C 5040                     00002168  1645+          STFPC FPC_R_20           save FPC
000021D2  E760 5028 080E                00002150  1646+          VST   V22,V1O20          save instruction result
000021D8  07FB                                    1647+          BR    R11                return
000021DC                                          1648+RE20      DS    0F                 expected 16 byte result
000021DC                                          1649+          DROP  R5
000021DC  4FFF8000 00000000                       1650           DC    XL16'4FFF8000000000000000000000000000'
000021E4  00000000 00000000
000021EC  7FFE0000 00000000                       1651           DC    XL16'7FFE0000000000000000000000000000'
000021F4  00000000 00000000
                                                  1652
                                                  1653 * min  dlfloat: 2^(-31)*+ulp
                                                  1654             VRR_A VCLFNH,2,0,00,00,N
00002200                                          1655+          DS    0FD
00002200                        00002200          1656+          USING *,R5               base for test data and test routine
00002200  00002290                                1657+T21       DC    A(X21)             address of test routine
00002204  0015                                    1658+          DC    H'21'              test number
00002206  00                                      1659+          DC    X'00'
00002207  D5                                      1660+          DC    CL1'N'             Y = skip cross check
00002208  02                                      1661+          DC    HL1'2'             m3
00002209  00                                      1662+          DC    HL1'0'             m4
0000220A  00                                      1663+FLG21     DC    X'00'              expected FPC flags
0000220B  00                                      1664+VXC21     DC    X'00'              expected VXC
0000220C  000022C4                                1665+V2_21     DC    A(RE21+16)         address of v2: 16-byte packed decimal
00002210  E5C3D3C6 D5C84040                       1666+          DC    CL8'VCLFNH'        instruction name
00002218  00000010                                1667+          DC    A(16)              result length
0000221C  000022B4                                1668+          DC    A(RE21)            address of expected resul
00002220  00000000 00000000                       1669+          DS    FD                 gap
00002228  00000000 00000000                       1670+V1O21     DS    XL16               V1 output
00002230  00000000 00000000
00002238  00000000 00000000                       1671+          DS    FD                   gap
00002240  00000000                                1672+FPC_R_21  DS    F                  FPC after instruction
00002248  00000000 00000000                       1673+          DS    FD                   gap
00002250  40404040 40404040                       1674+          DC    CL8' '             was cross check skipped?
00002258  00000000 00000000                       1675+          DS    FD                   gap
00002260  00000000 00000000                       1676+XCO21     DS    XL16               Cross check Output
00002268  00000000 00000000
00002270  00000000 00000000                       1677+          DS    FD                   gap
00002278  00000000                                1678+FPC_XC_21 DS    F                  FPC after cross check
00002280  00000000 00000000                       1679+          DS    FD                   gap
00002288  00000000                                1680+          DS    F                  debug area
0000228C  00000000                                1681+          DS    F
                                                  1682+*
00002290                                          1683+X21       DS    0F
00002290  B29D 84C4                     000006C4  1684+          LFPC  FPCINIT            initialize FPC
00002294  E320 A00C 0014                0000220C  1685+          LGF   R2,V2_21           get v2
0000229A  E762 0000 0806                00000000  1686+          VL    V22,0(R2)
000022A0  E666 0000 2C56                          1687+          VCLFNH V22,V22,2,0       test instruction (dest is source)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000022A6  B29C A040                     00002240  1688+         STFPC FPC_R_21          save FPC
000022AA  E760 A028 080E                00002228  1689+         VST   V22,V1O21         save instruction result
000022B0  07FB                                    1690+         BR    R11               return
000022B4                                          1691+RE21     DS    0F                expected 16 byte result
000022B4                                          1692+         DROP  R5
000022B4  30004000 00000000                       1693          DC    XL16'30004000000000000000000000000000'
000022BC  00000000 00000000
000022C4  00010000 00000000                       1694          DC    XL16'00010000000000000000000000000000'
000022CC  00000000 00000000
                                                  1695
                                                  1696 *  +NAN -NAN (invalid op)
                                                  1697          VRR_A VCLFNH,2,0,80,21,S          skip xcheck - includes NAN
000022D8                                          1698+         DS    0FD
000022D8                        000022D8          1699+         USING *,R5              base for test data and test routine
000022D8  00002368                                1700+T22      DC    A(X22)            address of test routine
000022DC  0016                                    1701+         DC    H'22'             test number
000022DE  00                                      1702+         DC    X'00'
000022DF  E2                                      1703+         DC    CL1'S'            Y = skip cross check
000022E0  02                                      1704+         DC    HL1'2'            m3
000022E1  00                                      1705+         DC    HL1'0'            m4
000022E2  80                                      1706+FLG22    DC    X'80'             expected FPC flags
000022E3  21                                      1707+VXC22    DC    X'21'             expected VXC
000022E4  0000239C                                1708+V2_22    DC    A(RE22+16)        address of v2: 16-byte packed decimal
000022E8  E5C3D3C6 D5C84040                       1709+         DC    CL8'VCLFNH'       instruction name
000022F0  00000010                                1710+         DC    A(16)             result length
000022F4  0000238C                                1711+         DC    A(RE22)           address of expected resul
000022F8  00000000 00000000                       1712+         DS    FD                gap
00002300  00000000 00000000                       1713+V1O22    DS    XL16              V1 output
00002308  00000000 00000000
00002310  00000000 00000000                       1714+         DS    FD                   gap
00002318  00000000                                1715+FPC_R_22 DS    F                 FPC after instruction
00002320  00000000 00000000                       1716+         DS    FD                   gap
00002328  40404040 40404040                       1717+         DC    CL8' '            was cross check skipped?
00002330  00000000 00000000                       1718+         DS    FD                   gap
00002338  00000000 00000000                       1719+XCO22    DS    XL16              Cross check Output
00002340  00000000 00000000
00002348  00000000 00000000                       1720+         DS    FD                   gap
00002350  00000000                                1721+FPC_XC_22 DS   F                 FPC after cross check
00002358  00000000 00000000                       1722+         DS    FD                   gap
00002360  00000000                                1723+         DS    F                 debug area
00002364  00000000                                1724+         DS    F
                                                  1725+*
00002368                                          1726+X22      DS    0F
00002368  B29D 84C4                     000006C4  1727+         LFPC  FPCINIT           initialize FPC
0000236C  E320 500C 0014                000022E4  1728+         LGF   R2,V2_22          get v2
00002372  E762 0000 0806                00000000  1729+         VL    V22,0(R2)
00002378  E666 0000 2C56                          1730+         VCLFNH V22,V22,2,0      test instruction (dest is source)
0000237E  B29C 5040                     00002318  1731+         STFPC FPC_R_22          save FPC
00002382  E760 5028 080E                00002300  1732+         VST   V22,V1O22         save instruction result
00002388  07FB                                    1733+         BR    R11               return
0000238C                                          1734+RE22     DS    0F                expected 16 byte result
0000238C                                          1735+         DROP  R5
0000238C  7FC00000 00000000                       1736          DC    XL16'7FC0000000000000FFC0000000000000'
00002394  FFC00000 00000000
0000239C  7FFF0000 FFFF0000                       1737          DC    XL16'7FFF0000FFFF00000000000000000000'
000023A4  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    1738
                                                    1739 * inexact - bad m3
                                                    1740          VRR_A VCLFNH,5,0,08,05,S                    skip xc - inexact
000023B0                                            1741+         DS    0FD
000023B0                        000023B0            1742+         USING *,R5              base for test data and test routine
000023B0  00002440                                  1743+T23      DC    A(X23)            address of test routine
000023B4  0017                                      1744+         DC    H'23'             test number
000023B6  00                                        1745+         DC    X'00'
000023B7  E2                                        1746+         DC    CL1'S'            Y = skip cross check
000023B8  05                                        1747+         DC    HL1'5'            m3
000023B9  00                                        1748+         DC    HL1'0'            m4
000023BA  08                                        1749+FLG23    DC    X'08'             expected FPC flags
000023BB  05                                        1750+VXC23    DC    X'05'             expected VXC
000023BC  00002474                                  1751+V2_23    DC    A(RE23+16)        address of v2: 16-byte packed decimal
000023C0  E5C3D3C6 D5C84040                         1752+         DC    CL8'VCLFNH'       instruction name
000023C8  00000010                                  1753+         DC    A(16)             result length
000023CC  00002464                                  1754+         DC    A(RE23)           address of expected resul
000023D0  00000000 00000000                         1755+         DS    FD                gap
000023D8  00000000 00000000                         1756+V1O23    DS    XL16              V1 output
000023E0  00000000 00000000
000023E8  00000000 00000000                         1757+         DS    FD                   gap
000023F0  00000000                                  1758+FPC_R_23 DS    F                 FPC after instruction
000023F8  00000000 00000000                         1759+         DS    FD                   gap
00002400  40404040 40404040                         1760+         DC    CL8' '            was cross check skipped?
00002408  00000000 00000000                         1761+         DS    FD                   gap
00002410  00000000 00000000                         1762+XCO23    DS    XL16              Cross check Output
00002418  00000000 00000000
00002420  00000000 00000000                         1763+         DS    FD                   gap
00002428  00000000                                  1764+FPC_XC_23 DS   F                 FPC after cross check
00002430  00000000 00000000                         1765+         DS    FD                   gap
00002438  00000000                                  1766+         DS    F                 debug area
0000243C  00000000                                  1767+         DS    F
                                                    1768+*
00002440                                            1769+X23      DS    0F
00002440  B29D 84C4                     000006C4    1770+         LFPC  FPCINIT           initialize FPC
00002444  E320 500C 0014                000023BC    1771+         LGF   R2,V2_23          get v2
0000244A  E762 0000 0806                00000000    1772+         VL    V22,0(R2)
00002450  E666 0000 5C56                            1773+         VCLFNH V22,V22,5,0      test instruction (dest is source)
00002456  B29C 5040                     000023F0    1774+         STFPC FPC_R_23          save FPC
0000245A  E760 5028 080E                000023D8    1775+         VST   V22,V1O23         save instruction result
00002460  07FB                                      1776+         BR    R11               return
00002464                                            1777+RE23     DS    0F                expected 16 byte result
00002464                                            1778+         DROP  R5
00002464  00000000 00000000                         1779          DC    XL16'00000000000000000000000000000000'    not checked
0000246C  00000000 00000000
00002474  00010000 00000000                         1780          DC    XL16'00010000000000000000000000F000'
0000247C  00000000 0000F000
                                                    1781
                                                    1782 *-------------------------------------------------------------------
                                                    1783 *  VCFN     - VECTOR FP CONVERT FROM NNP
                                                    1784 *-------------------------------------------------------------------
                                                    1785 *  dlfloat -> tinyt float (with cross check: tiny float -> dlfloat)
                                                    1786 *
                                                    1787
                                                    1788 * +0, -0     simple instruction and 'test' test
                                                    1789          VRR_A VCFN,1,0,00,00,N
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002488                                          1790+          DS    0FD
00002488                      00002488            1791+          USING *,R5              base for test data and test routine
00002488  00002518                                1792+T24       DC    A(X24)            address of test routine
0000248C  0018                                    1793+          DC    H'24'             test number
0000248E  00                                      1794+          DC    X'00'
0000248F  D5                                      1795+          DC    CL1'N'            Y = skip cross check
00002490  01                                      1796+          DC    HL1'1'            m3
00002491  00                                      1797+          DC    HL1'0'            m4
00002492  00                                      1798+FLG24     DC    X'00'             expected FPC flags
00002493  00                                      1799+VXC24     DC    X'00'             expected VXC
00002494  0000254C                                1800+V2_24     DC    A(RE24+16)        address of v2: 16-byte packed decimal
00002498  E5C3C6D5 40404040                       1801+          DC    CL8'VCFN'         instruction name
000024A0  00000010                                1802+          DC    A(16)             result length
000024A4  0000253C                                1803+          DC    A(RE24)           address of expected resul
000024A8  00000000 00000000                       1804+          DS    FD                gap
000024B0  00000000 00000000                       1805+V1O24     DS    XL16              V1 output
000024B8  00000000 00000000
000024C0  00000000 00000000                       1806+          DS    FD                   gap
000024C8  00000000                                1807+FPC_R_24  DS    F                 FPC after instruction
000024D0  00000000 00000000                       1808+          DS    FD                   gap
000024D8  40404040 40404040                       1809+          DC    CL8' '            was cross check skipped?
000024E0  00000000 00000000                       1810+          DS    FD                   gap
000024E8  00000000 00000000                       1811+XCO24     DS    XL16              Cross check Output
000024F0  00000000 00000000
000024F8  00000000 00000000                       1812+          DS    FD                   gap
00002500  00000000                                1813+FPC_XC_24 DS    F                 FPC after cross check
00002508  00000000 00000000                       1814+          DS    FD                   gap
00002510  00000000                                1815+          DS    F                 debug area
00002514  00000000                                1816+          DS    F
                                                  1817+*
00002518                                          1818+X24       DS    0F
00002518  B29D 84C4                     000006C4  1819+          LFPC  FPCINIT           initialize FPC
0000251C  E320 500C 0014                00002494  1820+          LGF   R2,V2_24          get v2
00002522  E762 0000 0806                00000000  1821+          VL    V22,0(R2)
00002528  E666 0000 1C5D                          1822+          VCFN  V22,V22,1,0       test instruction (dest is source)
0000252E  B29C 5040                     000024C8  1823+          STFPC FPC_R_24          save FPC
00002532  E760 5028 080E                000024B0  1824+          VST   V22,V1O24         save instruction result
00002538  07FB                                    1825+          BR    R11               return
0000253C                                          1826+RE24      DS    0F                expected 16 byte result
0000253C                                          1827+          DROP  R5
0000253C  00008000 00000000                       1828           DC    XL16'00008000000000000000000000000000'
00002544  00000000 00000000
0000254C  00008000 00000000                       1829           DC    XL16'00008000000000000000000000000000'
00002554  00000000 00000000
                                                  1830
                                                  1831 * 1.0, -1
                                                  1832           VRR_A VCFN,1,0,00,00,N
00002560                                          1833+          DS    0FD
00002560                      00002560            1834+          USING *,R5              base for test data and test routine
00002560  000025F0                                1835+T25       DC    A(X25)            address of test routine
00002564  0019                                    1836+          DC    H'25'             test number
00002566  00                                      1837+          DC    X'00'
00002567  D5                                      1838+          DC    CL1'N'            Y = skip cross check
00002568  01                                      1839+          DC    HL1'1'            m3
00002569  00                                      1840+          DC    HL1'0'            m4
0000256A  00                                      1841+FLG25     DC    X'00'             expected FPC flags
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
0000256B  00                                      1842+VXC25    DC    X'00'              expected VXC
0000256C  00002624                                1843+V2_25    DC    A(RE25+16)         address of v2: 16-byte packed decimal
00002570  E5C3C6D5 40404040                       1844+         DC    CL8'VCFN'          instruction name
00002578  00000010                                1845+         DC    A(16)              result length
0000257C  00002614                                1846+         DC    A(RE25)            address of expected resul
00002580  00000000 00000000                       1847+         DS    FD                 gap
00002588  00000000 00000000                       1848+V1O25    DS    XL16               V1 output
00002590  00000000 00000000
00002598  00000000 00000000                       1849+         DS    FD                    gap
000025A0  00000000                                1850+FPC_R_25 DS    F                  FPC after instruction
000025A8  00000000 00000000                       1851+         DS    FD                    gap
000025B0  40404040 40404040                       1852+         DC    CL8' '             was cross check skipped?
000025B8  00000000 00000000                       1853+         DS    FD                    gap
000025C0  00000000 00000000                       1854+XCO25    DS    XL16               Cross check Output
000025C8  00000000 00000000
000025D0  00000000 00000000                       1855+         DS    FD                    gap
000025D8  00000000                                1856+FPC_XC_25 DS   F                  FPC after cross check
000025E0  00000000 00000000                       1857+         DS    FD                    gap
000025E8  00000000                                1858+         DS    F                  debug area
000025EC  00000000                                1859+         DS    F
                                                  1860+*
000025F0                                          1861+X25      DS    0F
000025F0  B29D 84C4                     000006C4  1862+         LFPC  FPCINIT            initialize FPC
000025F4  E320 500C 0014                0000256C  1863+         LGF   R2,V2_25           get v2
000025FA  E762 0000 0806                00000000  1864+         VL    V22,0(R2)
00002600  E666 0000 1C5D                          1865+         VCFN  V22,V22,1,0        test instruction (dest is source)
00002606  B29C 5040                     000025A0  1866+         STFPC FPC_R_25           save FPC
0000260A  E760 5028 080E                00002588  1867+         VST   V22,V1O25          save instruction result
00002610  07FB                                    1868+         BR    R11                return
00002614                                          1869+RE25     DS    0F                 expected 16 byte result
00002614                                          1870+         DROP  R5
00002614  3C000000 BC000000                       1871          DC    XL16'3C000000BC000000000000000000F000'
0000261C  00000000 0000F000
00002624  3E000000 BE000000                       1872          DC    XL16'3E000000BE000000000000000000D800'
0000262C  00000000 0000D800
                                                  1873
                                                  1874 * 0.5
                                                  1875          VRR_A VCFN,1,0,00,00,N
00002638                                          1876+         DS    0FD
00002638                  00002638                1877+         USING *,R5               base for test data and test routine
00002638  000026C8                                1878+T26      DC    A(X26)             address of test routine
0000263C  001A                                    1879+         DC    H'26'              test number
0000263E  00                                      1880+         DC    X'00'
0000263F  D5                                      1881+         DC    CL1'N'             Y = skip cross check
00002640  01                                      1882+         DC    HL1'1'             m3
00002641  00                                      1883+         DC    HL1'0'             m4
00002642  00                                      1884+FLG26    DC    X'00'              expected FPC flags
00002643  00                                      1885+VXC26    DC    X'00'              expected VXC
00002644  000026FC                                1886+V2_26    DC    A(RE26+16)         address of v2: 16-byte packed decimal
00002648  E5C3C6D5 40404040                       1887+         DC    CL8'VCFN'          instruction name
00002650  00000010                                1888+         DC    A(16)              result length
00002654  000026EC                                1889+         DC    A(RE26)            address of expected resul
00002658  00000000 00000000                       1890+         DS    FD                 gap
00002660  00000000 00000000                       1891+V1O26    DS    XL16               V1 output
00002668  00000000 00000000
00002670  00000000 00000000                       1892+         DS    FD                    gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002678  00000000                                1893+FPC_R_26 DS    F                 FPC after instruction
00002680  00000000 00000000                       1894+         DS    FD                   gap
00002688  40404040 40404040                       1895+         DC    CL8' '            was cross check skipped?
00002690  00000000 00000000                       1896+         DS    FD                   gap
00002698  00000000 00000000                       1897+XCO26    DS    XL16              Cross check Output
000026A0  00000000 00000000
000026A8  00000000 00000000                       1898+         DS    FD                   gap
000026B0  00000000                                1899+FPC_XC_26 DS   F                 FPC after cross check
000026B8  00000000 00000000                       1900+         DS    FD                   gap
000026C0  00000000                                1901+         DS    F                 debug area
000026C4  00000000                                1902+         DS    F
                                                  1903+*
000026C8                                          1904+X26      DS    0F
000026C8  B29D 84C4                      000006C4 1905+         LFPC  FPCINIT           initialize FPC
000026CC  E320 500C 0014                 00002644 1906+         LGF   R2,V2_26          get v2
000026D2  E762 0000 0806                 00000000 1907+         VL    V22,0(R2)
000026D8  E666 0000 1C5D                          1908+         VCFN  V22,V22,1,0       test instruction (dest is source)
000026DE  B29C 5040                      00002678 1909+         STFPC FPC_R_26          save FPC
000026E2  E760 5028 080E                 00002660 1910+         VST   V22,V1O26         save instruction result
000026E8  07FB                                    1911+         BR    R11               return
000026EC                                          1912+RE26     DS    0F                expected 16 byte result
000026EC                                          1913+         DROP  R5
000026EC  38000000 00000000                       1914          DC    XL16'380000000000000000000000000F000'
000026F4  00000000 0000F000
000026FC  3C000000 00000000                       1915          DC    XL16'3C0000000000000000000000000D800'
00002704  00000000 0000D800
                                                  1916
                                                  1917 * 1/64
                                                  1918          VRR_A VCFN,1,0,00,00,N
00002710                                          1919+         DS    0FD
00002710                  00002710                1920+         USING *,R5              base for test data and test routine
00002710  000027A0                                1921+T27      DC    A(X27)            address of test routine
00002714  001B                                    1922+         DC    H'27'             test number
00002716  00                                      1923+         DC    X'00'
00002717  D5                                      1924+         DC    CL1'N'            Y = skip cross check
00002718  01                                      1925+         DC    HL1'1'            m3
00002719  00                                      1926+         DC    HL1'0'            m4
0000271A  00                                      1927+FLG27    DC    X'00'             expected FPC flags
0000271B  00                                      1928+VXC27    DC    X'00'             expected VXC
0000271C  000027D4                                1929+V2_27    DC    A(RE27+16)        address of v2: 16-byte packed decimal
00002720  E5C3C6D5 40404040                       1930+         DC    CL8'VCFN'         instruction name
00002728  00000010                                1931+         DC    A(16)             result length
0000272C  000027C4                                1932+         DC    A(RE27)           address of expected resul
00002730  00000000 00000000                       1933+         DS    FD                gap
00002738  00000000 00000000                       1934+V1O27    DS    XL16              V1 output
00002740  00000000 00000000
00002748  00000000 00000000                       1935+         DS    FD                   gap
00002750  00000000                                1936+FPC_R_27 DS    F                 FPC after instruction
00002758  00000000 00000000                       1937+         DS    FD                   gap
00002760  40404040 40404040                       1938+         DC    CL8' '            was cross check skipped?
00002768  00000000 00000000                       1939+         DS    FD                   gap
00002770  00000000 00000000                       1940+XCO27    DS    XL16              Cross check Output
00002778  00000000 00000000
00002780  00000000 00000000                       1941+         DS    FD                   gap
00002788  00000000                                1942+FPC_XC_27 DS   F                 FPC after cross check
00002790  00000000 00000000                       1943+         DS    FD                   gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002798  00000000                                1944+          DS    F                 debug area
0000279C  00000000                                1945+          DS    F
                                                  1946+*
000027A0                                          1947+X27       DS    0F
000027A0  B29D 84C4                     000006C4  1948+          LFPC  FPCINIT           initialize FPC
000027A4  E320 500C 0014                0000271C  1949+          LGF   R2,V2_27          get v2
000027AA  E762 0000 0806                00000000  1950+          VL    V22,0(R2)
000027B0  E666 0000 1C5D                          1951+          VCFN  V22,V22,1,0       test instruction (dest is source)
000027B6  B29C 5040                     00002750  1952+          STFPC FPC_R_27          save FPC
000027BA  E760 5028 080E                00002738  1953+          VST   V22,V1O27         save instruction result
000027C0  07FB                                    1954+          BR    R11               return
000027C4                                          1955+RE27      DS    0F                expected 16 byte result
000027C4                                          1956+          DROP  R5
000027C4  24000000 00000000                       1957           DC    XL16'240000000000000000000000000F000'
000027CC  00000000 0000F000
000027D4  32000000 00000000                       1958           DC    XL16'320000000000000000000000000D800'
000027DC  00000000 0000D800
                                                  1959
                                                  1960 * +0, -0
                                                  1961           VRR_A VCFN,1,0,00,00,N
000027E8                                          1962+          DS    0FD
000027E8                  000027E8                1963+          USING *,R5              base for test data and test routine
000027E8  00002878                                1964+T28       DC    A(X28)            address of test routine
000027EC  001C                                    1965+          DC    H'28'             test number
000027EE  00                                      1966+          DC    X'00'
000027EF  D5                                      1967+          DC    CL1'N'            Y = skip cross check
000027F0  01                                      1968+          DC    HL1'1'            m3
000027F1  00                                      1969+          DC    HL1'0'            m4
000027F2  00                                      1970+FLG28     DC    X'00'             expected FPC flags
000027F3  00                                      1971+VXC28     DC    X'00'             expected VXC
000027F4  000028AC                                1972+V2_28     DC    A(RE28+16)        address of v2: 16-byte packed decimal
000027F8  E5C3C6D5 40404040                       1973+          DC    CL8'VCFN'         instruction name
00002800  00000010                                1974+          DC    A(16)             result length
00002804  0000289C                                1975+          DC    A(RE28)           address of expected resul
00002808  00000000 00000000                       1976+          DS    FD                gap
00002810  00000000 00000000                       1977+V1O28     DS    XL16              V1 output
00002818  00000000 00000000
00002820  00000000 00000000                       1978+          DS    FD                   gap
00002828  00000000                                1979+FPC_R_28  DS    F                 FPC after instruction
00002830  00000000 00000000                       1980+          DS    FD                   gap
00002838  40404040 40404040                       1981+          DC    CL8' '            was cross check skipped?
00002840  00000000 00000000                       1982+          DS    FD                   gap
00002848  00000000 00000000                       1983+XCO28     DS    XL16              Cross check Output
00002850  00000000 00000000
00002858  00000000 00000000                       1984+          DS    FD                   gap
00002860  00000000                                1985+FPC_XC_28 DS    F                 FPC after cross check
00002868  00000000 00000000                       1986+          DS    FD                   gap
00002870  00000000                                1987+          DS    F                 debug area
00002874  00000000                                1988+          DS    F
                                                  1989+*
00002878                                          1990+X28       DS    0F
00002878  B29D 84C4                     000006C4  1991+          LFPC  FPCINIT           initialize FPC
0000287C  E320 500C 0014                000027F4  1992+          LGF   R2,V2_28          get v2
00002882  E762 0000 0806                00000000  1993+          VL    V22,0(R2)
00002888  E666 0000 1C5D                          1994+          VCFN  V22,V22,1,0       test instruction (dest is source)
0000288E  B29C 5040                     00002828  1995+          STFPC FPC_R_28          save FPC
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002892  E760 5028 080E                 00002810  1996+          VST   V22,V1O28         save instruction result
00002898  07FB                                     1997+          BR    R11               return
0000289C                                           1998+RE28      DS    0F                expected 16 byte result
0000289C                                           1999+          DROP  R5
0000289C  00008000 00000000                        2000           DC    XL16'00008000000000000000000000000F000'
000028A4  00000000 0000F000
000028AC  00008000 00000000                        2001           DC    XL16'00008000000000000000000000000D800'
000028B4  00000000 0000D800
                                                   2002
                                                   2003 * -15
                                                   2004           VRR_A VCFN,1,0,00,00,N
000028C0                                           2005+          DS    0FD
000028C0                  000028C0                 2006+          USING *,R5              base for test data and test routine
000028C0  00002950                                 2007+T29       DC    A(X29)            address of test routine
000028C4  001D                                     2008+          DC    H'29'             test number
000028C6  00                                       2009+          DC    X'00'
000028C7  D5                                       2010+          DC    CL1'N'            Y = skip cross check
000028C8  01                                       2011+          DC    HL1'1'            m3
000028C9  00                                       2012+          DC    HL1'0'            m4
000028CA  00                                       2013+FLG29     DC    X'00'             expected FPC flags
000028CB  00                                       2014+VXC29     DC    X'00'             expected VXC
000028CC  00002984                                 2015+V2_29     DC    A(RE29+16)        address of v2: 16-byte packed decimal
000028D0  E5C3C6D5 40404040                        2016+          DC    CL8'VCFN'         instruction name
000028D8  00000010                                 2017+          DC    A(16)             result length
000028DC  00002974                                 2018+          DC    A(RE29)           address of expected resul
000028E0  00000000 00000000                        2019+          DS    FD                gap
000028E8  00000000 00000000                        2020+V1O29     DS    XL16              V1 output
000028F0  00000000 00000000
000028F8  00000000 00000000                        2021+          DS    FD                   gap
00002900  00000000                                 2022+FPC_R_29  DS    F                 FPC after instruction
00002908  00000000 00000000                        2023+          DS    FD                   gap
00002910  40404040 40404040                        2024+          DC    CL8' '            was cross check skipped?
00002918  00000000 00000000                        2025+          DS    FD                   gap
00002920  00000000 00000000                        2026+XCO29     DS    XL16              Cross check Output
00002928  00000000 00000000
00002930  00000000 00000000                        2027+          DS    FD                   gap
00002938  00000000                                 2028+FPC_XC_29 DS    F                 FPC after cross check
00002940  00000000 00000000                        2029+          DS    FD                   gap
00002948  00000000                                 2030+          DS    F                 debug area
0000294C  00000000                                 2031+          DS    F
                                                   2032+*
00002950                                           2033+X29       DS    0F
00002950  B29D 84C4                       000006C4 2034+          LFPC  FPCINIT           initialize FPC
00002954  E320 500C 0014                  000028CC 2035+          LGF   R2,V2_29          get v2
0000295A  E762 0000 0806                  00000000 2036+          VL    V22,0(R2)
00002960  E666 0000 1C5D                           2037+          VCFN  V22,V22,1,0       test instruction (dest is source)
00002966  B29C 5040                       00002900 2038+          STFPC FPC_R_29          save FPC
0000296A  E760 5028 080E                  000028E8 2039+          VST   V22,V1O29         save instruction result
00002970  07FB                                     2040+          BR    R11               return
00002974                                           2041+RE29      DS    0F                expected 16 byte result
00002974                                           2042+          DROP  R5
00002974  CB800000 00000000                        2043           DC    XL16'CB80000000000000000000000000F000'
0000297C  00000000 0000F000
00002984  C5C00000 00000000                        2044           DC    XL16'C5C00000000000000000000000000D800'
0000298C  00000000 0000D800
                                                   2045
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   2046 * 20/7 (about)
                                                   2047          VRR_A VCFN,1,0,00,00,N
00002998                                           2048+         DS    0FD
00002998                       00002998            2049+         USING *,R5              base for test data and test routine
00002998  00002A28                                 2050+T30      DC    A(X30)            address of test routine
0000299C  001E                                     2051+         DC    H'30'             test number
0000299E  00                                       2052+         DC    X'00'
0000299F  D5                                       2053+         DC    CL1'N'            Y = skip cross check
000029A0  01                                       2054+         DC    HL1'1'            m3
000029A1  00                                       2055+         DC    HL1'0'            m4
000029A2  00                                       2056+FLG30    DC    X'00'             expected FPC flags
000029A3  00                                       2057+VXC30    DC    X'00'             expected VXC
000029A4  00002A5C                                 2058+V2_30    DC    A(RE30+16)        address of v2: 16-byte packed decimal
000029A8  E5C3C6D5 40404040                        2059+         DC    CL8'VCFN'         instruction name
000029B0  00000010                                 2060+         DC    A(16)             result length
000029B4  00002A4C                                 2061+         DC    A(RE30)           address of expected resul
000029B8  00000000 00000000                        2062+         DS    FD                gap
000029C0  00000000 00000000                        2063+V1O30    DS    XL16              V1 output
000029C8  00000000 00000000
000029D0  00000000 00000000                        2064+         DS    FD                   gap
000029D8  00000000                                 2065+FPC_R_30 DS    F                 FPC after instruction
000029E0  00000000 00000000                        2066+         DS    FD                   gap
000029E8  40404040 40404040                        2067+         DC    CL8' '            was cross check skipped?
000029F0  00000000 00000000                        2068+         DS    FD                   gap
000029F8  00000000 00000000                        2069+XCO30    DS    XL16              Cross check Output
00002A00  00000000 00000000
00002A08  00000000 00000000                        2070+         DS    FD                   gap
00002A10  00000000                                 2071+FPC_XC_30 DS   F                 FPC after cross check
00002A18  00000000 00000000                        2072+         DS    FD                   gap
00002A20  00000000                                 2073+         DS    F                 debug area
00002A24  00000000                                 2074+         DS    F
                                                   2075+*
00002A28                                           2076+X30      DS    0F
00002A28  B29D 84C4                     000006C4   2077+         LFPC  FPCINIT           initialize FPC
00002A2C  E320 500C 0014                000029A4   2078+         LGF   R2,V2_30          get v2
00002A32  E762 0000 0806                00000000   2079+         VL    V22,0(R2)
00002A38  E666 0000 1C5D                           2080+         VCFN  V22,V22,1,0       test instruction (dest is source)
00002A3E  B29C 5040                     000029D8   2081+         STFPC FPC_R_30          save FPC
00002A42  E760 5028 080E                000029C0   2082+         VST   V22,V1O30         save instruction result
00002A48  07FB                                     2083+         BR    R11               return
00002A4C                                           2084+RE30     DS    0F                expected 16 byte result
00002A4C                                           2085+         DROP  R5
00002A4C  41B60000 00000000                        2086          DC    XL16'41B60000000000000000000000F000'
00002A54  00000000 0000F000
00002A5C  40DB0000 00000000                        2087          DC    XL16'40DB0000000000000000000000D800'
00002A64  00000000 0000D800
                                                   2088
                                                   2089 * additional tests
                                                   2090 * max  tiny:  (1 - 2^-11) * 2^16 (65504) +1 (overflow)
                                                   2091          VRR_A VCFN,1,0,20,03,S
00002A70                                           2092+         DS    0FD
00002A70                       00002A70            2093+         USING *,R5              base for test data and test routine
00002A70  00002B00                                 2094+T31      DC    A(X31)            address of test routine
00002A74  001F                                     2095+         DC    H'31'             test number
00002A76  00                                       2096+         DC    X'00'
00002A77  E2                                       2097+         DC    CL1'S'            Y = skip cross check
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002A78  01                                      2098+          DC    HL1'1'            m3
00002A79  00                                      2099+          DC    HL1'0'            m4
00002A7A  20                                      2100+FLG31     DC    X'20'             expected FPC flags
00002A7B  03                                      2101+VXC31     DC    X'03'             expected VXC
00002A7C  00002B34                                2102+V2_31     DC    A(RE31+16)        address of v2: 16-byte packed decimal
00002A80  E5C3C6D5 40404040                       2103+          DC    CL8'VCFN'         instruction name
00002A88  00000010                                2104+          DC    A(16)             result length
00002A8C  00002B24                                2105+          DC    A(RE31)           address of expected resul
00002A90  00000000 00000000                       2106+          DS    FD                gap
00002A98  00000000 00000000                       2107+V1O31     DS    XL16              V1 output
00002AA0  00000000 00000000
00002AA8  00000000 00000000                       2108+          DS    FD                   gap
00002AB0  00000000                                2109+FPC_R_31  DS    F                 FPC after instruction
00002AB8  00000000 00000000                       2110+          DS    FD                   gap
00002AC0  40404040 40404040                       2111+          DC    CL8' '            was cross check skipped?
00002AC8  00000000 00000000                       2112+          DS    FD                   gap
00002AD0  00000000 00000000                       2113+XCO31     DS    XL16              Cross check Output
00002AD8  00000000 00000000
00002AE0  00000000 00000000                       2114+          DS    FD                   gap
00002AE8  00000000                                2115+FPC_XC_31 DS    F                 FPC after cross check
00002AF0  00000000 00000000                       2116+          DS    FD                   gap
00002AF8  00000000                                2117+          DS    F                 debug area
00002AFC  00000000                                2118+          DS    F
                                                  2119+*
00002B00                                          2120+X31       DS    0F
00002B00  B29D 84C4                     000006C4  2121+          LFPC  FPCINIT           initialize FPC
00002B04  E320 500C 0014                00002A7C  2122+          LGF   R2,V2_31          get v2
00002B0A  E762 0000 0806                00000000  2123+          VL    V22,0(R2)
00002B10  E666 0000 1C5D                          2124+          VCFN  V22,V22,1,0       test instruction (dest is source)
00002B16  B29C 5040                     00002AB0  2125+          STFPC FPC_R_31          save FPC
00002B1A  E760 5028 080E                00002A98  2126+          VST   V22,V1O31         save instruction result
00002B20  07FB                                    2127+          BR    R11               return
00002B24                                          2128+RE31      DS    0F                expected 16 byte result
00002B24                                          2129+          DROP  R5
00002B24  7C000000 00000000                       2130           DC    XL16'7C000000000000000000000000F000'
00002B2C  00000000 0000F000
00002B34  5E000000 00000000                       2131           DC    XL16'5E000000000000000000000000D800'
00002B3C  00000000 0000D800
                                                  2132
                                                  2133
                                                  2134 * min tiny (normal): 2^-14 (0.00006103515625)
                                                  2135           VRR_A VCFN,1,0,00,00,N
00002B48                                          2136+          DS    0FD
00002B48                        00002B48          2137+          USING *,R5              base for test data and test routine
00002B48  00002BD8                                2138+T32       DC    A(X32)            address of test routine
00002B4C  0020                                    2139+          DC    H'32'             test number
00002B4E  00                                      2140+          DC    X'00'
00002B4F  D5                                      2141+          DC    CL1'N'            Y = skip cross check
00002B50  01                                      2142+          DC    HL1'1'            m3
00002B51  00                                      2143+          DC    HL1'0'            m4
00002B52  00                                      2144+FLG32     DC    X'00'             expected FPC flags
00002B53  00                                      2145+VXC32     DC    X'00'             expected VXC
00002B54  00002C0C                                2146+V2_32     DC    A(RE32+16)        address of v2: 16-byte packed decimal
00002B58  E5C3C6D5 40404040                       2147+          DC    CL8'VCFN'         instruction name
00002B60  00000010                                2148+          DC    A(16)             result length
00002B64  00002BFC                                2149+          DC    A(RE32)           address of expected resul
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002B68  00000000 00000000                      2150+          DS    FD                gap
00002B70  00000000 00000000                      2151+V1O32     DS    XL16              V1 output
00002B78  00000000 00000000
00002B80  00000000 00000000                      2152+          DS    FD                   gap
00002B88  00000000                               2153+FPC_R_32  DS    F                 FPC after instruction
00002B90  00000000 00000000                      2154+          DS    FD                   gap
00002B98  40404040 40404040                      2155+          DC    CL8' '            was cross check skipped?
00002BA0  00000000 00000000                      2156+          DS    FD                   gap
00002BA8  00000000 00000000                      2157+XCO32     DS    XL16              Cross check Output
00002BB0  00000000 00000000
00002BB8  00000000 00000000                      2158+          DS    FD                   gap
00002BC0  00000000                               2159+FPC_XC_32 DS    F                 FPC after cross check
00002BC8  00000000 00000000                      2160+          DS    FD                   gap
00002BD0  00000000                               2161+          DS    F                 debug area
00002BD4  00000000                               2162+          DS    F
                                                 2163+*
00002BD8                                         2164+X32       DS    0F
00002BD8  B29D 84C4                   000006C4   2165+          LFPC  FPCINIT           initialize FPC
00002BDC  E320 500C 0014              00002B54   2166+          LGF   R2,V2_32          get v2
00002BE2  E762 0000 0806              00000000   2167+          VL    V22,0(R2)
00002BE8  E666 0000 1C5D                         2168+          VCFN  V22,V22,1,0       test instruction (dest is source)
00002BEE  B29C 5040                   00002B88   2169+          STFPC FPC_R_32          save FPC
00002BF2  E760 5028 080E              00002B70   2170+          VST   V22,V1O32         save instruction result
00002BF8  07FB                                   2171+          BR    R11               return
00002BFC                                         2172+RE32      DS    0F                expected 16 byte result
00002BFC                                         2173+          DROP  R5
00002BFC  04000000 00000000                      2174           DC    XL16'040000000000000000000000000F000'
00002C04  00000000 0000F000
00002C0C  22000000 00000000                      2175           DC    XL16'220000000000000000000000000D800'
00002C14  00000000 0000D800
                                                 2176
                                                 2177 * min tiny (subnormal): 2^-24 (0.00000005960464477539062 5)
                                                 2178           VRR_A VCFN,1,0,00,00,N
00002C20                                         2179+          DS    0FD
00002C20                      00002C20           2180+          USING *,R5              base for test data and test routine
00002C20  00002CB0                               2181+T33       DC    A(X33)            address of test routine
00002C24  0021                                   2182+          DC    H'33'             test number
00002C26  00                                     2183+          DC    X'00'
00002C27  D5                                     2184+          DC    CL1'N'            Y = skip cross check
00002C28  01                                     2185+          DC    HL1'1'            m3
00002C29  00                                     2186+          DC    HL1'0'            m4
00002C2A  00                                     2187+FLG33     DC    X'00'             expected FPC flags
00002C2B  00                                     2188+VXC33     DC    X'00'             expected VXC
00002C2C  00002CE4                               2189+V2_33     DC    A(RE33+16)        address of v2: 16-byte packed decimal
00002C30  E5C3C6D5 40404040                      2190+          DC    CL8'VCFN'         instruction name
00002C38  00000010                               2191+          DC    A(16)             result length
00002C3C  00002CD4                               2192+          DC    A(RE33)           address of expected resul
00002C40  00000000 00000000                      2193+          DS    FD                gap
00002C48  00000000 00000000                      2194+V1O33     DS    XL16              V1 output
00002C50  00000000 00000000
00002C58  00000000 00000000                      2195+          DS    FD                   gap
00002C60  00000000                               2196+FPC_R_33  DS    F                 FPC after instruction
00002C68  00000000 00000000                      2197+          DS    FD                   gap
00002C70  40404040 40404040                      2198+          DC    CL8' '            was cross check skipped?
00002C78  00000000 00000000                      2199+          DS    FD                   gap
00002C80  00000000 00000000                      2200+XCO33     DS    XL16              Cross check Output
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002C88  00000000 00000000
00002C90  00000000 00000000                        2201+          DS    FD                   gap
00002C98  00000000                                 2202+FPC_XC_33 DS    F                  FPC after cross check
00002CA0  00000000 00000000                        2203+          DS    FD                   gap
00002CA8  00000000                                 2204+          DS    F                  debug area
00002CAC  00000000                                 2205+          DS    F
                                                   2206+*
00002CB0                                           2207+X33       DS    0F
00002CB0  B29D 84C4                      000006C4  2208+          LFPC  FPCINIT            initialize FPC
00002CB4  E320 500C 0014                 00002C2C  2209+          LGF   R2,V2_33           get v2
00002CBA  E762 0000 0806                 00000000  2210+          VL    V22,0(R2)
00002CC0  E666 0000 1C5D                           2211+          VCFN  V22,V22,1,0        test instruction (dest is source)
00002CC6  B29C 5040                      00002C60  2212+          STFPC FPC_R_33           save FPC
00002CCA  E760 5028 080E                 00002C48  2213+          VST   V22,V1O33          save instruction result
00002CD0  07FB                                     2214+          BR    R11                return
00002CD4                                           2215+RE33      DS    0F                 expected 16 byte result
00002CD4                                           2216+          DROP  R5
00002CD4  00010000 00000000                        2217           DC    XL16'00010000000000000000000000000F000'
00002CDC  00000000 0000F000
00002CE4  0E000000 00000000                        2218           DC    XL16'0E000000000000000000000000000D800'
00002CEC  00000000 0000D800
                                                   2219
                                                   2220 *  2 underflows
                                                   2221           VRR_A VCFN,1,0,10,14,S
00002CF8                                           2222+          DS    0FD
00002CF8                         00002CF8          2223+          USING *,R5               base for test data and test routine
00002CF8  00002D88                                 2224+T34       DC    A(X34)             address of test routine
00002CFC  0022                                     2225+          DC    H'34'              test number
00002CFE  00                                       2226+          DC    X'00'
00002CFF  E2                                       2227+          DC    CL1'S'             Y = skip cross check
00002D00  01                                       2228+          DC    HL1'1'             m3
00002D01  00                                       2229+          DC    HL1'0'             m4
00002D02  10                                       2230+FLG34     DC    X'10'              expected FPC flags
00002D03  14                                       2231+VXC34     DC    X'14'              expected VXC
00002D04  00002DBC                                 2232+V2_34     DC    A(RE34+16)         address of v2: 16-byte packed decimal
00002D08  E5C3C6D5 40404040                        2233+          DC    CL8'VCFN'          instruction name
00002D10  00000010                                 2234+          DC    A(16)              result length
00002D14  00002DAC                                 2235+          DC    A(RE34)            address of expected resul
00002D18  00000000 00000000                        2236+          DS    FD                 gap
00002D20  00000000 00000000                        2237+V1O34     DS    XL16               V1 output
00002D28  00000000 00000000
00002D30  00000000 00000000                        2238+          DS    FD                   gap
00002D38  00000000                                 2239+FPC_R_34  DS    F                  FPC after instruction
00002D40  00000000 00000000                        2240+          DS    FD                   gap
00002D48  40404040 40404040                        2241+          DC    CL8' '             was cross check skipped?
00002D50  00000000 00000000                        2242+          DS    FD                   gap
00002D58  00000000 00000000                        2243+XCO34     DS    XL16               Cross check Output
00002D60  00000000 00000000
00002D68  00000000 00000000                        2244+          DS    FD                   gap
00002D70  00000000                                 2245+FPC_XC_34 DS    F                  FPC after cross check
00002D78  00000000 00000000                        2246+          DS    FD                   gap
00002D80  00000000                                 2247+          DS    F                  debug area
00002D84  00000000                                 2248+          DS    F
                                                   2249+*
00002D88                                           2250+X34       DS    0F
00002D88  B29D 84C4                      000006C4  2251+          LFPC  FPCINIT            initialize FPC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00002D8C  E320 500C 0014                 00002D04  2252+          LGF   R2,V2_34          get v2
00002D92  E762 0000 0806                 00000000  2253+          VL    V22,0(R2)
00002D98  E666 0000 1C5D                           2254+          VCFN  V22,V22,1,0       test instruction (dest is source)
00002D9E  B29C 5040                      00002D38  2255+          STFPC FPC_R_34          save FPC
00002DA2  E760 5028 080E                 00002D20  2256+          VST   V22,V1O34         save instruction result
00002DA8  07FB                                     2257+          BR    R11               return
00002DAC                                           2258+RE34      DS    0F                expected 16 byte result
00002DAC                                           2259+          DROP  R5
00002DAC  00000000 00000000                        2260           DC    XL16'0000000000000000000000000000F000'
00002DB4  00000000 0000F000
00002DBC  0A000B00 00000000                        2261           DC    XL16'0A000B0000000000000000000000D800'
00002DC4  00000000 0000D800
                                                   2262
                                                   2263 * NAN,
                                                   2264           VRR_A VCFN,1,0,80,01,S                  invalip op: NAN-> ?
00002DD0                                           2265+          DS    0FD
00002DD0                           00002DD0        2266+          USING *,R5              base for test data and test routine
00002DD0  00002E60                                 2267+T35       DC    A(X35)            address of test routine
00002DD4  0023                                     2268+          DC    H'35'             test number
00002DD6  00                                       2269+          DC    X'00'
00002DD7  E2                                       2270+          DC    CL1'S'            Y = skip cross check
00002DD8  01                                       2271+          DC    HL1'1'            m3
00002DD9  00                                       2272+          DC    HL1'0'            m4
00002DDA  80                                       2273+FLG35     DC    X'80'             expected FPC flags
00002DDB  01                                       2274+VXC35     DC    X'01'             expected VXC
00002DDC  00002E94                                 2275+V2_35     DC    A(RE35+16)        address of v2: 16-byte packed decimal
00002DE0  E5C3C6D5 40404040                        2276+          DC    CL8'VCFN'         instruction name
00002DE8  00000010                                 2277+          DC    A(16)             result length
00002DEC  00002E84                                 2278+          DC    A(RE35)           address of expected resul
00002DF0  00000000 00000000                        2279+          DS    FD                gap
00002DF8  00000000 00000000                        2280+V1O35     DS    XL16              V1 output
00002E00  00000000 00000000
00002E08  00000000 00000000                        2281+          DS    FD                   gap
00002E10  00000000                                 2282+FPC_R_35  DS    F                 FPC after instruction
00002E18  00000000 00000000                        2283+          DS    FD                   gap
00002E20  40404040 40404040                        2284+          DC    CL8' '            was cross check skipped?
00002E28  00000000 00000000                        2285+          DS    FD                   gap
00002E30  00000000 00000000                        2286+XCO35     DS    XL16              Cross check Output
00002E38  00000000 00000000
00002E40  00000000 00000000                        2287+          DS    FD                   gap
00002E48  00000000                                 2288+FPC_XC_35 DS    F                 FPC after cross check
00002E50  00000000 00000000                        2289+          DS    FD                   gap
00002E58  00000000                                 2290+          DS    F                 debug area
00002E5C  00000000                                 2291+          DS    F
                                                   2292+*
00002E60                                           2293+X35       DS    0F
00002E60  B29D 84C4                      000006C4  2294+          LFPC  FPCINIT           initialize FPC
00002E64  E320 500C 0014                 00002DDC  2295+          LGF   R2,V2_35          get v2
00002E6A  E762 0000 0806                 00000000  2296+          VL    V22,0(R2)
00002E70  E666 0000 1C5D                           2297+          VCFN  V22,V22,1,0       test instruction (dest is source)
00002E76  B29C 5040                      00002E10  2298+          STFPC FPC_R_35          save FPC
00002E7A  E760 5028 080E                 00002DF8  2299+          VST   V22,V1O35         save instruction result
00002E80  07FB                                     2300+          BR    R11               return
00002E84                                           2301+RE35      DS    0F                expected 16 byte result
00002E84                                           2302+          DROP  R5
00002E84  FE000000 00000000                        2303           DC    XL16'FE0000000000000000000000000F000'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002E8C  00000000 0000F000
00002E94  FFFF0000 00000000                        2304          DC    XL16'FFFF0000000000000000000000D800'
00002E9C  00000000 0000D800
                                                   2305
                                                   2306 * inexact - bad m3
                                                   2307          VRR_A VCFN,5,0,08,05,S                    skip xc - inexact
00002EA8                                           2308+         DS    0FD
00002EA8                      00002EA8             2309+         USING *,R5              base for test data and test routine
00002EA8  00002F38                                 2310+T36      DC    A(X36)            address of test routine
00002EAC  0024                                     2311+         DC    H'36'             test number
00002EAE  00                                       2312+         DC    X'00'
00002EAF  E2                                       2313+         DC    CL1'S'            Y = skip cross check
00002EB0  05                                       2314+         DC    HL1'5'            m3
00002EB1  00                                       2315+         DC    HL1'0'            m4
00002EB2  08                                       2316+FLG36    DC    X'08'             expected FPC flags
00002EB3  05                                       2317+VXC36    DC    X'05'             expected VXC
00002EB4  00002F6C                                 2318+V2_36    DC    A(RE36+16)        address of v2: 16-byte packed decimal
00002EB8  E5C3C6D5 40404040                        2319+         DC    CL8'VCFN'         instruction name
00002EC0  00000010                                 2320+         DC    A(16)             result length
00002EC4  00002F5C                                 2321+         DC    A(RE36)           address of expected resul
00002EC8  00000000 00000000                        2322+         DS    FD                gap
00002ED0  00000000 00000000                        2323+V1O36    DS    XL16              V1 output
00002ED8  00000000 00000000
00002EE0  00000000 00000000                        2324+         DS    FD                   gap
00002EE8  00000000                                 2325+FPC_R_36 DS    F                 FPC after instruction
00002EF0  00000000 00000000                        2326+         DS    FD                   gap
00002EF8  40404040 40404040                        2327+         DC    CL8' '            was cross check skipped?
00002F00  00000000 00000000                        2328+         DS    FD                   gap
00002F08  00000000 00000000                        2329+XCO36    DS    XL16              Cross check Output
00002F10  00000000 00000000
00002F18  00000000 00000000                        2330+         DS    FD                   gap
00002F20  00000000                                 2331+FPC_XC_36 DS   F                 FPC after cross check
00002F28  00000000 00000000                        2332+         DS    FD                   gap
00002F30  00000000                                 2333+         DS    F                 debug area
00002F34  00000000                                 2334+         DS    F
                                                   2335+*
00002F38                                           2336+X36      DS    0F
00002F38  B29D 84C4                     000006C4   2337+         LFPC  FPCINIT           initialize FPC
00002F3C  E320 500C 0014                00002EB4   2338+         LGF   R2,V2_36          get v2
00002F42  E762 0000 0806                00000000   2339+         VL    V22,0(R2)
00002F48  E666 0000 5C5D                           2340+         VCFN  V22,V22,5,0       test instruction (dest is source)
00002F4E  B29C 5040                     00002EE8   2341+         STFPC FPC_R_36          save FPC
00002F52  E760 5028 080E                00002ED0   2342+         VST   V22,V1O36         save instruction result
00002F58  07FB                                     2343+         BR    R11               return
00002F5C                                           2344+RE36     DS    0F                expected 16 byte result
00002F5C                                           2345+         DROP  R5
00002F5C  00000000 00000000                        2346          DC    XL16'00000000000000000000000000000000'    not checked
00002F64  00000000 00000000
00002F6C  00010000 00000000                        2347          DC    XL16'00010000000000000000000000F000'
00002F74  00000000 0000F000
                                                   2348
                                                   2349 *-------------------------------------------------------------------
                                                   2350 * VCLFNL   - VECTOR FP CONVERT AND LENGTHEN FROM NNP LOW
                                                   2351 *-------------------------------------------------------------------
                                                   2352 *  dlfloat -> short float (with cross check: short float -> dlfloat)
                                                   2353 *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    2354
                                                    2355 * +0, -0     simple instruction and 'test' test
                                                    2356          VRR_A VCLFNL,2,0,00,00,N
00002F80                                            2357+         DS    0FD
00002F80                      00002F80              2358+         USING *,R5              base for test data and test routine
00002F80  00003010                                  2359+T37      DC    A(X37)            address of test routine
00002F84  0025                                      2360+         DC    H'37'             test number
00002F86  00                                        2361+         DC    X'00'
00002F87  D5                                        2362+         DC    CL1'N'            Y = skip cross check
00002F88  02                                        2363+         DC    HL1'2'            m3
00002F89  00                                        2364+         DC    HL1'0'            m4
00002F8A  00                                        2365+FLG37    DC    X'00'             expected FPC flags
00002F8B  00                                        2366+VXC37    DC    X'00'             expected VXC
00002F8C  00003044                                  2367+V2_37    DC    A(RE37+16)        address of v2: 16-byte packed decimal
00002F90  E5C3D3C6 D5D34040                         2368+         DC    CL8'VCLFNL'       instruction name
00002F98  00000010                                  2369+         DC    A(16)             result length
00002F9C  00003034                                  2370+         DC    A(RE37)           address of expected resul
00002FA0  00000000 00000000                         2371+         DS    FD                gap
00002FA8  00000000 00000000                         2372+V1O37    DS    XL16              V1 output
00002FB0  00000000 00000000
00002FB8  00000000 00000000                         2373+         DS    FD                   gap
00002FC0  00000000                                  2374+FPC_R_37 DS    F                 FPC after instruction
00002FC8  00000000 00000000                         2375+         DS    FD                   gap
00002FD0  40404040 40404040                         2376+         DC    CL8' '            was cross check skipped?
00002FD8  00000000 00000000                         2377+         DS    FD                   gap
00002FE0  00000000 00000000                         2378+XCO37    DS    XL16              Cross check Output
00002FE8  00000000 00000000
00002FF0  00000000 00000000                         2379+         DS    FD                   gap
00002FF8  00000000                                  2380+FPC_XC_37 DS   F                 FPC after cross check
00003000  00000000 00000000                         2381+         DS    FD                   gap
00003008  00000000                                  2382+         DS    F                 debug area
0000300C  00000000                                  2383+         DS    F
                                                    2384+*
00003010                                            2385+X37      DS    0F
00003010  B29D 84C4                       000006C4  2386+         LFPC  FPCINIT           initialize FPC
00003014  E320 500C 0014                  00002F8C  2387+         LGF   R2,V2_37          get v2
0000301A  E762 0000 0806                  00000000  2388+         VL    V22,0(R2)
00003020  E666 0000 2C5E                            2389+         VCLFNL V22,V22,2,0      test instruction (dest is source)
00003026  B29C 5040                       00002FC0  2390+         STFPC FPC_R_37          save FPC
0000302A  E760 5028 080E                  00002FA8  2391+         VST   V22,V1O37         save instruction result
00003030  07FB                                      2392+         BR    R11               return
00003034                                            2393+RE37     DS    0F                expected 16 byte result
00003034                                            2394+         DROP  R5
00003034  00000000 80000000                         2395          DC    XL16'00000000800000000000000000000000'
0000303C  00000000 00000000
00003044  00000000 00000000                         2396          DC    XL16'00000000000000000000800000000000'
0000304C  00008000 00000000
                                                    2397
                                                    2398 * +1, -1
                                                    2399          VRR_A VCLFNL,2,0,00,00,N
00003058                                            2400+         DS    0FD
00003058                      00003058              2401+         USING *,R5              base for test data and test routine
00003058  000030E8                                  2402+T38      DC    A(X38)            address of test routine
0000305C  0026                                      2403+         DC    H'38'             test number
0000305E  00                                        2404+         DC    X'00'
0000305F  D5                                        2405+         DC    CL1'N'            Y = skip cross check
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003060  02                                      2406+          DC    HL1'2'            m3
00003061  00                                      2407+          DC    HL1'0'            m4
00003062  00                                      2408+FLG38     DC    X'00'             expected FPC flags
00003063  00                                      2409+VXC38     DC    X'00'             expected VXC
00003064  0000311C                                2410+V2_38     DC    A(RE38+16)        address of v2: 16-byte packed decimal
00003068  E5C3D3C6 D5D34040                       2411+          DC    CL8'VCLFNL'       instruction name
00003070  00000010                                2412+          DC    A(16)             result length
00003074  0000310C                                2413+          DC    A(RE38)           address of expected resul
00003078  00000000 00000000                       2414+          DS    FD                gap
00003080  00000000 00000000                       2415+V1O38     DS    XL16              V1 output
00003088  00000000 00000000
00003090  00000000 00000000                       2416+          DS    FD                   gap
00003098  00000000                                2417+FPC_R_38  DS    F                 FPC after instruction
000030A0  00000000 00000000                       2418+          DS    FD                   gap
000030A8  40404040 40404040                       2419+          DC    CL8' '            was cross check skipped?
000030B0  00000000 00000000                       2420+          DS    FD                   gap
000030B8  00000000 00000000                       2421+XCO38     DS    XL16              Cross check Output
000030C0  00000000 00000000
000030C8  00000000 00000000                       2422+          DS    FD                   gap
000030D0  00000000                                2423+FPC_XC_38 DS    F                 FPC after cross check
000030D8  00000000 00000000                       2424+          DS    FD                   gap
000030E0  00000000                                2425+          DS    F                 debug area
000030E4  00000000                                2426+          DS    F
                                                  2427+*
000030E8                                          2428+X38       DS    0F
000030E8  B29D 84C4                     000006C4  2429+          LFPC  FPCINIT           initialize FPC
000030EC  E320 500C 0014                00003064  2430+          LGF   R2,V2_38          get v2
000030F2  E762 0000 0806                00000000  2431+          VL    V22,0(R2)
000030F8  E666 0000 2C5E                          2432+          VCLFNL V22,V22,2,0      test instruction (dest is source)
000030FE  B29C 5040                     00003098  2433+          STFPC FPC_R_38          save FPC
00003102  E760 5028 080E                00003080  2434+          VST   V22,V1O38         save instruction result
00003108  07FB                                    2435+          BR    R11               return
0000310C                                          2436+RE38      DS    0F                expected 16 byte result
0000310C                                          2437+          DROP  R5
0000310C  3F800000 BF800000                       2438           DC    XL16'3F800000BF800000000000000000000000'
00003114  00000000 00000000
0000311C  00000000 00000000                       2439           DC    XL16'0000000000000003E00BE0000000000'
00003124  3E00BE00 00000000
                                                  2440
                                                  2441 * +0.5, -0.5
                                                  2442           VRR_A VCLFNL,2,0,00,00,N
00003130                                          2443+          DS    0FD
00003130                  00003130                2444+          USING *,R5              base for test data and test routine
00003130  000031C0                                2445+T39       DC    A(X39)            address of test routine
00003134  0027                                    2446+          DC    H'39'             test number
00003136  00                                      2447+          DC    X'00'
00003137  D5                                      2448+          DC    CL1'N'            Y = skip cross check
00003138  02                                      2449+          DC    HL1'2'            m3
00003139  00                                      2450+          DC    HL1'0'            m4
0000313A  00                                      2451+FLG39     DC    X'00'             expected FPC flags
0000313B  00                                      2452+VXC39     DC    X'00'             expected VXC
0000313C  000031F4                                2453+V2_39     DC    A(RE39+16)        address of v2: 16-byte packed decimal
00003140  E5C3D3C6 D5D34040                       2454+          DC    CL8'VCLFNL'       instruction name
00003148  00000010                                2455+          DC    A(16)             result length
0000314C  000031E4                                2456+          DC    A(RE39)           address of expected resul
00003150  00000000 00000000                       2457+          DS    FD                gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003158  00000000 00000000                        2458+V1O39    DS    XL16              V1 output
00003160  00000000 00000000
00003168  00000000 00000000                        2459+         DS    FD                   gap
00003170  00000000                                 2460+FPC_R_39 DS    F                 FPC after instruction
00003178  00000000 00000000                        2461+         DS    FD                   gap
00003180  40404040 40404040                        2462+         DC    CL8' '            was cross check skipped?
00003188  00000000 00000000                        2463+         DS    FD                   gap
00003190  00000000 00000000                        2464+XCO39    DS    XL16              Cross check Output
00003198  00000000 00000000
000031A0  00000000 00000000                        2465+         DS    FD                   gap
000031A8  00000000                                 2466+FPC_XC_39 DS   F                 FPC after cross check
000031B0  00000000 00000000                        2467+         DS    FD                   gap
000031B8  00000000                                 2468+         DS    F                 debug area
000031BC  00000000                                 2469+         DS    F
                                                   2470+*
000031C0                                           2471+X39      DS    0F
000031C0  B29D 84C4                      000006C4  2472+         LFPC  FPCINIT           initialize FPC
000031C4  E320 500C 0014                 0000313C  2473+         LGF   R2,V2_39          get v2
000031CA  E762 0000 0806                 00000000  2474+         VL    V22,0(R2)
000031D0  E666 0000 2C5E                           2475+         VCLFNL V22,V22,2,0      test instruction (dest is source)
000031D6  B29C 5040                      00003170  2476+         STFPC FPC_R_39          save FPC
000031DA  E760 5028 080E                 00003158  2477+         VST   V22,V1O39         save instruction result
000031E0  07FB                                     2478+         BR    R11               return
000031E4                                           2479+RE39     DS    0F                expected 16 byte result
000031E4                                           2480+         DROP  R5
000031E4  3F000000 BF000000                        2481          DC    XL16'3F000000BF000000000000000000000000'
000031EC  00000000 00000000
000031F4  00000000 00000000                        2482          DC    XL16'0000000000000003C00BC0000000000'
000031FC  3C00BC00 00000000
                                                   2483
                                                   2484 * 1/64, -1/64
                                                   2485          VRR_A VCLFNL,2,0,00,00,N
00003208                                           2486+         DS    0FD
00003208                       00003208            2487+         USING *,R5              base for test data and test routine
00003208  00003298                                 2488+T40      DC    A(X40)            address of test routine
0000320C  0028                                     2489+         DC    H'40'             test number
0000320E  00                                       2490+         DC    X'00'
0000320F  D5                                       2491+         DC    CL1'N'            Y = skip cross check
00003210  02                                       2492+         DC    HL1'2'            m3
00003211  00                                       2493+         DC    HL1'0'            m4
00003212  00                                       2494+FLG40    DC    X'00'             expected FPC flags
00003213  00                                       2495+VXC40    DC    X'00'             expected VXC
00003214  000032CC                                 2496+V2_40    DC    A(RE40+16)        address of v2: 16-byte packed decimal
00003218  E5C3D3C6 D5D34040                        2497+         DC    CL8'VCLFNL'       instruction name
00003220  00000010                                 2498+         DC    A(16)             result length
00003224  000032BC                                 2499+         DC    A(RE40)           address of expected resul
00003228  00000000 00000000                        2500+         DS    FD                gap
00003230  00000000 00000000                        2501+V1O40    DS    XL16              V1 output
00003238  00000000 00000000
00003240  00000000 00000000                        2502+         DS    FD                   gap
00003248  00000000                                 2503+FPC_R_40 DS    F                 FPC after instruction
00003250  00000000 00000000                        2504+         DS    FD                   gap
00003258  40404040 40404040                        2505+         DC    CL8' '            was cross check skipped?
00003260  00000000 00000000                        2506+         DS    FD                   gap
00003268  00000000 00000000                        2507+XCO40    DS    XL16              Cross check Output
00003270  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003278  00000000 00000000                        2508+          DS    FD                   gap
00003280  00000000                                 2509+FPC_XC_40 DS    F                  FPC after cross check
00003288  00000000 00000000                        2510+          DS    FD                   gap
00003290  00000000                                 2511+          DS    F                  debug area
00003294  00000000                                 2512+          DS    F
                                                   2513+*
00003298                                           2514+X40       DS    0F
00003298  B29D 84C4                      000006C4  2515+          LFPC  FPCINIT            initialize FPC
0000329C  E320 500C 0014                 00003214  2516+          LGF   R2,V2_40           get v2
000032A2  E762 0000 0806                 00000000  2517+          VL    V22,0(R2)
000032A8  E666 0000 2C5E                           2518+          VCLFNL V22,V22,2,0       test instruction (dest is source)
000032AE  B29C 5040                      00003248  2519+          STFPC FPC_R_40           save FPC
000032B2  E760 5028 080E                 00003230  2520+          VST   V22,V1O40          save instruction result
000032B8  07FB                                     2521+          BR    R11                return
000032BC                                           2522+RE40      DS    0F                 expected 16 byte result
000032BC                                           2523+          DROP  R5
000032BC  3C800000 BC800000                        2524           DC    XL16'3C800000BC80000000000000000000000'
000032C4  00000000 00000000
000032CC  00000000 00000000                        2525           DC    XL16'00000000000000003200B20000000000'
000032D4  3200B200 00000000
                                                   2526
                                                   2527 * +15, -15
                                                   2528           VRR_A VCLFNL,2,0,00,00,N
000032E0                                           2529+          DS    0FD
000032E0                 000032E0                  2530+          USING *,R5               base for test data and test routine
000032E0  00003370                                 2531+T41       DC    A(X41)             address of test routine
000032E4  0029                                     2532+          DC    H'41'              test number
000032E6  00                                       2533+          DC    X'00'
000032E7  D5                                       2534+          DC    CL1'N'             Y = skip cross check
000032E8  02                                       2535+          DC    HL1'2'             m3
000032E9  00                                       2536+          DC    HL1'0'             m4
000032EA  00                                       2537+FLG41     DC    X'00'              expected FPC flags
000032EB  00                                       2538+VXC41     DC    X'00'              expected VXC
000032EC  000033A4                                 2539+V2_41     DC    A(RE41+16)         address of v2: 16-byte packed decimal
000032F0  E5C3D3C6 D5D34040                        2540+          DC    CL8'VCLFNL'        instruction name
000032F8  00000010                                 2541+          DC    A(16)              result length
000032FC  00003394                                 2542+          DC    A(RE41)            address of expected resul
00003300  00000000 00000000                        2543+          DS    FD                 gap
00003308  00000000 00000000                        2544+V1O41     DS    XL16               V1 output
00003310  00000000 00000000
00003318  00000000 00000000                        2545+          DS    FD                   gap
00003320  00000000                                 2546+FPC_R_41  DS    F                  FPC after instruction
00003328  00000000 00000000                        2547+          DS    FD                   gap
00003330  40404040 40404040                        2548+          DC    CL8' '             was cross check skipped?
00003338  00000000 00000000                        2549+          DS    FD                   gap
00003340  00000000 00000000                        2550+XCO41     DS    XL16               Cross check Output
00003348  00000000 00000000
00003350  00000000 00000000                        2551+          DS    FD                   gap
00003358  00000000                                 2552+FPC_XC_41 DS    F                  FPC after cross check
00003360  00000000 00000000                        2553+          DS    FD                   gap
00003368  00000000                                 2554+          DS    F                  debug area
0000336C  00000000                                 2555+          DS    F
                                                   2556+*
00003370                                           2557+X41       DS    0F
00003370  B29D 84C4                      000006C4  2558+          LFPC  FPCINIT            initialize FPC
00003374  E320 500C 0014                 000032EC  2559+          LGF   R2,V2_41           get v2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
0000337A  E762 0000 0806                 00000000  2560+         VL    V22,0(R2)
00003380  E666 0000 2C5E                           2561+         VCLFNL V22,V22,2,0      test instruction (dest is source)
00003386  B29C 5040                      00003320  2562+         STFPC FPC_R_41          save FPC
0000338A  E760 5028 080E                 00003308  2563+         VST   V22,V1O41         save instruction result
00003390  07FB                                     2564+         BR    R11               return
00003394                                           2565+RE41     DS    0F                expected 16 byte result
00003394                                           2566+         DROP  R5
00003394  41700000 C1700000                        2567          DC    XL16'41700000C1700000000000000000000'
0000339C  00000000 00000000
000033A4  00000000 00000000                        2568          DC    XL16'0000000000000000045C0C5C000000000'
000033AC  45C0C5C0 00000000
                                                   2569
                                                   2570 * +20/7, -20/7 (about)
                                                   2571          VRR_A VCLFNL,2,0,00,00,N
000033B8                                           2572+         DS    0FD
000033B8                 000033B8                  2573+         USING *,R5              base for test data and test routine
000033B8  00003448                                 2574+T42      DC    A(X42)            address of test routine
000033BC  002A                                     2575+         DC    H'42'             test number
000033BE  00                                       2576+         DC    X'00'
000033BF  D5                                       2577+         DC    CL1'N'            Y = skip cross check
000033C0  02                                       2578+         DC    HL1'2'            m3
000033C1  00                                       2579+         DC    HL1'0'            m4
000033C2  00                                       2580+FLG42    DC    X'00'             expected FPC flags
000033C3  00                                       2581+VXC42    DC    X'00'             expected VXC
000033C4  0000347C                                 2582+V2_42    DC    A(RE42+16)        address of v2: 16-byte packed decimal
000033C8  E5C3D3C6 D5D34040                        2583+         DC    CL8'VCLFNL'       instruction name
000033D0  00000010                                 2584+         DC    A(16)             result length
000033D4  0000346C                                 2585+         DC    A(RE42)           address of expected resul
000033D8  00000000 00000000                        2586+         DS    FD                gap
000033E0  00000000 00000000                        2587+V1O42    DS    XL16              V1 output
000033E8  00000000 00000000
000033F0  00000000 00000000                        2588+         DS    FD                   gap
000033F8  00000000                                 2589+FPC_R_42 DS    F                 FPC after instruction
00003400  00000000 00000000                        2590+         DS    FD                   gap
00003408  40404040 40404040                        2591+         DC    CL8' '            was cross check skipped?
00003410  00000000 00000000                        2592+         DS    FD                   gap
00003418  00000000 00000000                        2593+XCO42    DS    XL16              Cross check Output
00003420  00000000 00000000
00003428  00000000 00000000                        2594+         DS    FD                   gap
00003430  00000000                                 2595+FPC_XC_42 DS   F                 FPC after cross check
00003438  00000000 00000000                        2596+         DS    FD                   gap
00003440  00000000                                 2597+         DS    F                 debug area
00003444  00000000                                 2598+         DS    F
                                                   2599+*
00003448                                           2600+X42      DS    0F
00003448  B29D 84C4                      000006C4  2601+         LFPC  FPCINIT           initialize FPC
0000344C  E320 500C 0014                 000033C4  2602+         LGF   R2,V2_42          get v2
00003452  E762 0000 0806                 00000000  2603+         VL    V22,0(R2)
00003458  E666 0000 2C5E                           2604+         VCLFNL V22,V22,2,0      test instruction (dest is source)
0000345E  B29C 5040                      000033F8  2605+         STFPC FPC_R_42          save FPC
00003462  E760 5028 080E                 000033E0  2606+         VST   V22,V1O42         save instruction result
00003468  07FB                                     2607+         BR    R11               return
0000346C                                           2608+RE42     DS    0F                expected 16 byte result
0000346C                                           2609+         DROP  R5
0000346C  4036C000 C036C000                        2610          DC    XL16'4036C000C036C0000000000000000000'
00003474  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000347C  00000000 00000000                        2611          DC    XL16'00000000000000040DBC0DB00000000'
00003484  40DBC0DB 00000000                        
                                                   2612
                                                   2613 * additional tests
                                                   2614 * max  tiny:  (1 - 2^-11) * 2^16 (65504)
                                                   2615          VRR_A VCLFNL,2,0,00,00,N
00003490                                           2616+         DS    0FD
00003490                     00003490              2617+         USING *,R5              base for test data and test routine
00003490  00003520                                 2618+T43      DC    A(X43)            address of test routine
00003494  002B                                     2619+         DC    H'43'             test number
00003496  00                                       2620+         DC    X'00'
00003497  D5                                       2621+         DC    CL1'N'            Y = skip cross check
00003498  02                                       2622+         DC    HL1'2'            m3
00003499  00                                       2623+         DC    HL1'0'            m4
0000349A  00                                       2624+FLG43    DC    X'00'             expected FPC flags
0000349B  00                                       2625+VXC43    DC    X'00'             expected VXC
0000349C  00003554                                 2626+V2_43    DC    A(RE43+16)        address of v2: 16-byte packed decimal
000034A0  E5C3D3C6 D5D34040                        2627+         DC    CL8'VCLFNL'       instruction name
000034A8  00000010                                 2628+         DC    A(16)             result length
000034AC  00003544                                 2629+         DC    A(RE43)           address of expected resul
000034B0  00000000 00000000                        2630+         DS    FD                gap
000034B8  00000000 00000000                        2631+V1O43    DS    XL16              V1 output
000034C0  00000000 00000000
000034C8  00000000 00000000                        2632+         DS    FD                   gap
000034D0  00000000                                 2633+FPC_R_43 DS    F                 FPC after instruction
000034D8  00000000 00000000                        2634+         DS    FD                   gap
000034E0  40404040 40404040                        2635+         DC    CL8' '            was cross check skipped?
000034E8  00000000 00000000                        2636+         DS    FD                   gap
000034F0  00000000 00000000                        2637+XCO43    DS    XL16              Cross check Output
000034F8  00000000 00000000
00003500  00000000 00000000                        2638+         DS    FD                   gap
00003508  00000000                                 2639+FPC_XC_43 DS   F                 FPC after cross check
00003510  00000000 00000000                        2640+         DS    FD                   gap
00003518  00000000                                 2641+         DS    F                 debug area
0000351C  00000000                                 2642+         DS    F
                                                   2643+*
00003520                                           2644+X43      DS    0F
00003520  B29D 84C4                      000006C4  2645+         LFPC  FPCINIT           initialize FPC
00003524  E320 500C 0014                 0000349C  2646+         LGF   R2,V2_43          get v2
0000352A  E762 0000 0806                 00000000  2647+         VL    V22,0(R2)
00003530  E666 0000 2C5E                           2648+         VCLFNL V22,V22,2,0      test instruction (dest is source)
00003536  B29C 5040                      000034D0  2649+         STFPC FPC_R_43          save FPC
0000353A  E760 5028 080E                 000034B8  2650+         VST   V22,V1O43         save instruction result
00003540  07FB                                     2651+         BR    R11               return
00003544                                           2652+RE43     DS    0F                expected 16 byte result
00003544                                           2653+         DROP  R5
00003544  47800000 00000000                        2654          DC    XL16'47800000000000000000000000000000'
0000354C  00000000 00000000
00003554  00000000 00000000                        2655          DC    XL16'00000000000000005E00000000000000'
0000355C  5E000000 00000000
                                                   2656
                                                   2657 * max  dlfloat:  2^(33)-2ulp
                                                   2658          VRR_A VCLFNL,2,0,00,00,N
00003568                                           2659+         DS    0FD
00003568                     00003568              2660+         USING *,R5              base for test data and test routine
00003568  000035F8                                 2661+T44      DC    A(X44)            address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000356C  002C                                    2662+          DC    H'44'              test number
0000356E  00                                      2663+          DC    X'00'
0000356F  D5                                      2664+          DC    CL1'N'             Y = skip cross check
00003570  02                                      2665+          DC    HL1'2'             m3
00003571  00                                      2666+          DC    HL1'0'             m4
00003572  00                                      2667+FLG44     DC    X'00'              expected FPC flags
00003573  00                                      2668+VXC44     DC    X'00'              expected VXC
00003574  0000362C                                2669+V2_44     DC    A(RE44+16)         address of v2: 16-byte packed decimal
00003578  E5C3D3C6 D5D34040                       2670+          DC    CL8'VCLFNL'        instruction name
00003580  00000010                                2671+          DC    A(16)              result length
00003584  0000361C                                2672+          DC    A(RE44)            address of expected resul
00003588  00000000 00000000                       2673+          DS    FD                 gap
00003590  00000000 00000000                       2674+V1O44     DS    XL16               V1 output
00003598  00000000 00000000
000035A0  00000000 00000000                       2675+          DS    FD                    gap
000035A8  00000000                                2676+FPC_R_44  DS    F                  FPC after instruction
000035B0  00000000 00000000                       2677+          DS    FD                    gap
000035B8  40404040 40404040                       2678+          DC    CL8' '             was cross check skipped?
000035C0  00000000 00000000                       2679+          DS    FD                    gap
000035C8  00000000 00000000                       2680+XCO44     DS    XL16               Cross check Output
000035D0  00000000 00000000
000035D8  00000000 00000000                       2681+          DS    FD                    gap
000035E0  00000000                                2682+FPC_XC_44 DS    F                  FPC after cross check
000035E8  00000000 00000000                       2683+          DS    FD                    gap
000035F0  00000000                                2684+          DS    F                  debug area
000035F4  00000000                                2685+          DS    F
                                                  2686+*
000035F8                                          2687+X44       DS    0F
000035F8  B29D 84C4                     000006C4  2688+          LFPC  FPCINIT            initialize FPC
000035FC  E320 500C 0014                00003574  2689+          LGF   R2,V2_44           get v2
00003602  E762 0000 0806                00000000  2690+          VL    V22,0(R2)
00003608  E666 0000 2C5E                          2691+          VCLFNL V22,V22,2,0       test instruction (dest is source)
0000360E  B29C 5040                     000035A8  2692+          STFPC FPC_R_44           save FPC
00003612  E760 5028 080E                00003590  2693+          VST   V22,V1O44          save instruction result
00003618  07FB                                    2694+          BR    R11                return
0000361C                                          2695+RE44      DS    0F                 expected 16 byte result
0000361C                                          2696+          DROP  R5
0000361C  4FFF8000 00000000                       2697           DC    XL16'4FFF8000000000000000000000000000'
00003624  00000000 00000000
0000362C  00000000 00000000                       2698           DC    XL16'00000000000000007FFE000000000000'
00003634  7FFE0000 00000000
                                                  2699
                                                  2700 * min  dlfloat: 2^(-31)*+ulp
                                                  2701           VRR_A VCLFNL,2,0,00,00,N
00003640                                          2702+          DS    0FD
00003640                        00003640          2703+          USING *,R5               base for test data and test routine
00003640  000036D0                                2704+T45       DC    A(X45)             address of test routine
00003644  002D                                    2705+          DC    H'45'              test number
00003646  00                                      2706+          DC    X'00'
00003647  D5                                      2707+          DC    CL1'N'             Y = skip cross check
00003648  02                                      2708+          DC    HL1'2'             m3
00003649  00                                      2709+          DC    HL1'0'             m4
0000364A  00                                      2710+FLG45     DC    X'00'              expected FPC flags
0000364B  00                                      2711+VXC45     DC    X'00'              expected VXC
0000364C  00003704                                2712+V2_45     DC    A(RE45+16)         address of v2: 16-byte packed decimal
00003650  E5C3D3C6 D5D34040                       2713+          DC    CL8'VCLFNL'        instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003658  00000010                          2714+          DC    A(16)              result length
0000365C  000036F4                          2715+          DC    A(RE45)            address of expected resul
00003660  00000000 00000000                 2716+          DS    FD                 gap
00003668  00000000 00000000                 2717+V1O45     DS    XL16               V1 output
00003670  00000000 00000000
00003678  00000000 00000000                 2718+          DS    FD                    gap
00003680  00000000                          2719+FPC_R_45  DS    F                  FPC after instruction
00003688  00000000 00000000                 2720+          DS    FD                    gap
00003690  40404040 40404040                 2721+          DC    CL8' '             was cross check skipped?
00003698  00000000 00000000                 2722+          DS    FD                    gap
000036A0  00000000 00000000                 2723+XCO45     DS    XL16               Cross check Output
000036A8  00000000 00000000
000036B0  00000000 00000000                 2724+          DS    FD                    gap
000036B8  00000000                          2725+FPC_XC_45 DS    F                  FPC after cross check
000036C0  00000000 00000000                 2726+          DS    FD                    gap
000036C8  00000000                          2727+          DS    F                  debug area
000036CC  00000000                          2728+          DS    F
                                            2729+*
000036D0                                    2730+X45       DS    0F
000036D0  B29D 84C4                 000006C4 2731+          LFPC  FPCINIT            initialize FPC
000036D4  E320 500C 0014            0000364C 2732+          LGF   R2,V2_45           get v2
000036DA  E762 0000 0806            00000000 2733+          VL    V22,0(R2)
000036E0  E666 0000 2C5E                     2734+          VCLFNL V22,V22,2,0       test instruction (dest is source)
000036E6  B29C 5040                 00003680 2735+          STFPC FPC_R_45           save FPC
000036EA  E760 5028 080E            00003668 2736+          VST   V22,V1O45          save instruction result
000036F0  07FB                               2737+          BR    R11                return
000036F4                                    2738+RE45      DS    0F                 expected 16 byte result
000036F4                                    2739+          DROP  R5
000036F4  30004000 00000000                 2740           DC    XL16'30004000000000000000000000000000'
000036FC  00000000 00000000
00003704  00000000 00000000                 2741           DC    XL16'00000000000000000001000000000000'
0000370C  00010000 00000000
                                            2742
                                            2743 *  +NAN -NAN (invalid op)
                                            2744           VRR_A VCLFNL,2,0,80,61,S          skip xcheck - includes NAN
00003718                                    2745+          DS    0FD
00003718                    00003718        2746+          USING *,R5               base for test data and test routine
00003718  000037A8                          2747+T46       DC    A(X46)             address of test routine
0000371C  002E                              2748+          DC    H'46'              test number
0000371E  00                                2749+          DC    X'00'
0000371F  E2                                2750+          DC    CL1'S'             Y = skip cross check
00003720  02                                2751+          DC    HL1'2'             m3
00003721  00                                2752+          DC    HL1'0'             m4
00003722  80                                2753+FLG46     DC    X'80'              expected FPC flags
00003723  61                                2754+VXC46     DC    X'61'              expected VXC
00003724  000037DC                          2755+V2_46     DC    A(RE46+16)         address of v2: 16-byte packed decimal
00003728  E5C3D3C6 D5D34040                 2756+          DC    CL8'VCLFNL'        instruction name
00003730  00000010                          2757+          DC    A(16)              result length
00003734  000037CC                          2758+          DC    A(RE46)            address of expected resul
00003738  00000000 00000000                 2759+          DS    FD                 gap
00003740  00000000 00000000                 2760+V1O46     DS    XL16               V1 output
00003748  00000000 00000000
00003750  00000000 00000000                 2761+          DS    FD                    gap
00003758  00000000                          2762+FPC_R_46  DS    F                  FPC after instruction
00003760  00000000 00000000                 2763+          DS    FD                    gap
00003768  40404040 40404040                 2764+          DC    CL8' '             was cross check skipped?
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003770  00000000 00000000                       2765+          DS    FD                   gap
00003778  00000000 00000000                       2766+XCO46     DS    XL16               Cross check Output
00003780  00000000 00000000
00003788  00000000 00000000                       2767+          DS    FD                   gap
00003790  00000000                                2768+FPC_XC_46 DS    F                  FPC after cross check
00003798  00000000 00000000                       2769+          DS    FD                   gap
000037A0  00000000                                2770+          DS    F                  debug area
000037A4  00000000                                2771+          DS    F
                                                  2772+*
000037A8                                          2773+X46       DS    0F
000037A8  B29D 84C4                     000006C4  2774+          LFPC  FPCINIT            initialize FPC
000037AC  E320 500C 0014                00003724  2775+          LGF   R2,V2_46           get v2
000037B2  E762 0000 0806                00000000  2776+          VL    V22,0(R2)
000037B8  E666 0000 2C5E                          2777+          VCLFNL V22,V22,2,0       test instruction (dest is source)
000037BE  B29C 5040                     00003758  2778+          STFPC FPC_R_46           save FPC
000037C2  E760 5028 080E                00003740  2779+          VST   V22,V1O46          save instruction result
000037C8  07FB                                    2780+          BR    R11                return
000037CC                                          2781+RE46      DS    0F                 expected 16 byte result
000037CC                                          2782+          DROP  R5
000037CC  7FC00000 00000000                       2783           DC    XL16'7FC0000000000000FFC0000000000000'
000037D4  FFC00000 00000000
000037DC  00000000 00000000                       2784           DC    XL16'0000000000000007FFF0000FFFF0000'
000037E4  7FFF0000 FFFF0000
                                                  2785
                                                  2786 * inexact - bad m3
                                                  2787           VRR_A VCLFNL,5,0,08,05,S                  skip xc - inexact
000037F0                                          2788+          DS    0FD
000037F0                  000037F0                2789+          USING *,R5               base for test data and test routine
000037F0  00003880                                2790+T47       DC    A(X47)             address of test routine
000037F4  002F                                    2791+          DC    H'47'              test number
000037F6  00                                      2792+          DC    X'00'
000037F7  E2                                      2793+          DC    CL1'S'             Y = skip cross check
000037F8  05                                      2794+          DC    HL1'5'             m3
000037F9  00                                      2795+          DC    HL1'0'             m4
000037FA  08                                      2796+FLG47     DC    X'08'              expected FPC flags
000037FB  05                                      2797+VXC47     DC    X'05'              expected VXC
000037FC  000038B4                                2798+V2_47     DC    A(RE47+16)         address of v2: 16-byte packed decimal
00003800  E5C3D3C6 D5D34040                       2799+          DC    CL8'VCLFNL'        instruction name
00003808  00000010                                2800+          DC    A(16)              result length
0000380C  000038A4                                2801+          DC    A(RE47)            address of expected resul
00003810  00000000 00000000                       2802+          DS    FD                 gap
00003818  00000000 00000000                       2803+V1O47     DS    XL16               V1 output
00003820  00000000 00000000
00003828  00000000 00000000                       2804+          DS    FD                   gap
00003830  00000000                                2805+FPC_R_47  DS    F                  FPC after instruction
00003838  00000000 00000000                       2806+          DS    FD                   gap
00003840  40404040 40404040                       2807+          DC    CL8' '             was cross check skipped?
00003848  00000000 00000000                       2808+          DS    FD                   gap
00003850  00000000 00000000                       2809+XCO47     DS    XL16               Cross check Output
00003858  00000000 00000000
00003860  00000000 00000000                       2810+          DS    FD                   gap
00003868  00000000                                2811+FPC_XC_47 DS    F                  FPC after cross check
00003870  00000000 00000000                       2812+          DS    FD                   gap
00003878  00000000                                2813+          DS    F                  debug area
0000387C  00000000                                2814+          DS    F
                                                  2815+*
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
00003880                                          2816+X47      DS    0F
00003880  B29D 84C4                     000006C4  2817+          LFPC  FPCINIT           initialize FPC
00003884  E320 500C 0014                000037FC  2818+          LGF   R2,V2_47          get v2
0000388A  E762 0000 0806                00000000  2819+          VL    V22,0(R2)
00003890  E666 0000 5C5E                          2820+          VCLFNL V22,V22,5,0      test instruction (dest is source)
00003896  B29C 5040                     00003830  2821+          STFPC FPC_R_47          save FPC
0000389A  E760 5028 080E                00003818  2822+          VST   V22,V1O47         save instruction result
000038A0  07FB                                    2823+          BR    R11               return
000038A4                                          2824+RE47     DS    0F                expected 16 byte result
000038A4                                          2825+          DROP  R5
000038A4  00000000 00000000                       2826           DC    XL16'00000000000000000000000000000000'    not checked
000038AC  00000000 00000000
000038B4  00000000 0000F000                       2827           DC    XL16'000000000000F0000001000000000000'
000038BC  00010000 00000000
                                                  2828
                                                  2829
000038C4  00000000                                2830           DC    F'0'      END OF TABLE
000038C8  00000000                                2831           DC    F'0'
                                                  2832 *
                                                  2833 * table of pointers to individual tests
                                                  2834 *
000038CC                                          2835 E6TESTS  DS    0F
                                                  2836           PTTABLE
000038CC                                          2837+TTABLE   DS    0F
000038CC  00001120                                2838+          DC    A(T1)             TEST &CUR
000038D0  000011F8                                2839+          DC    A(T2)             TEST &CUR
000038D4  000012D0                                2840+          DC    A(T3)             TEST &CUR
000038D8  000013A8                                2841+          DC    A(T4)             TEST &CUR
000038DC  00001480                                2842+          DC    A(T5)             TEST &CUR
000038E0  00001558                                2843+          DC    A(T6)             TEST &CUR
000038E4  00001630                                2844+          DC    A(T7)             TEST &CUR
000038E8  00001708                                2845+          DC    A(T8)             TEST &CUR
000038EC  000017E0                                2846+          DC    A(T9)             TEST &CUR
000038F0  000018B8                                2847+          DC    A(T10)            TEST &CUR
000038F4  00001990                                2848+          DC    A(T11)            TEST &CUR
000038F8  00001A68                                2849+          DC    A(T12)            TEST &CUR
000038FC  00001B40                                2850+          DC    A(T13)            TEST &CUR
00003900  00001C18                                2851+          DC    A(T14)            TEST &CUR
00003904  00001CF0                                2852+          DC    A(T15)            TEST &CUR
00003908  00001DC8                                2853+          DC    A(T16)            TEST &CUR
0000390C  00001EA0                                2854+          DC    A(T17)            TEST &CUR
00003910  00001F78                                2855+          DC    A(T18)            TEST &CUR
00003914  00002050                                2856+          DC    A(T19)            TEST &CUR
00003918  00002128                                2857+          DC    A(T20)            TEST &CUR
0000391C  00002200                                2858+          DC    A(T21)            TEST &CUR
00003920  000022D8                                2859+          DC    A(T22)            TEST &CUR
00003924  000023B0                                2860+          DC    A(T23)            TEST &CUR
00003928  00002488                                2861+          DC    A(T24)            TEST &CUR
0000392C  00002560                                2862+          DC    A(T25)            TEST &CUR
00003930  00002638                                2863+          DC    A(T26)            TEST &CUR
00003934  00002710                                2864+          DC    A(T27)            TEST &CUR
00003938  000027E8                                2865+          DC    A(T28)            TEST &CUR
0000393C  000028C0                                2866+          DC    A(T29)            TEST &CUR
00003940  00002998                                2867+          DC    A(T30)            TEST &CUR
00003944  00002A70                                2868+          DC    A(T31)            TEST &CUR
00003948  00002B48                                2869+          DC    A(T32)            TEST &CUR
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000394C  00002C20                                2870+          DC    A(T33)             TEST &CUR
00003950  00002CF8                                2871+          DC    A(T34)             TEST &CUR
00003954  00002DD0                                2872+          DC    A(T35)             TEST &CUR
00003958  00002EA8                                2873+          DC    A(T36)             TEST &CUR
0000395C  00002F80                                2874+          DC    A(T37)             TEST &CUR
00003960  00003058                                2875+          DC    A(T38)             TEST &CUR
00003964  00003130                                2876+          DC    A(T39)             TEST &CUR
00003968  00003208                                2877+          DC    A(T40)             TEST &CUR
0000396C  000032E0                                2878+          DC    A(T41)             TEST &CUR
00003970  000033B8                                2879+          DC    A(T42)             TEST &CUR
00003974  00003490                                2880+          DC    A(T43)             TEST &CUR
00003978  00003568                                2881+          DC    A(T44)             TEST &CUR
0000397C  00003640                                2882+          DC    A(T45)             TEST &CUR
00003980  00003718                                2883+          DC    A(T46)             TEST &CUR
00003984  000037F0                                2884+          DC    A(T47)             TEST &CUR
                                                  2885+*
00003988  00000000                                2886+          DC    A(0)               END OF TABLE
0000398C  00000000                                2887+          DC    A(0)
                                                  2888
00003990  00000000                                2889           DC    F'0'      END OF TABLE
00003994  00000000                                2890           DC    F'0'
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                     2892 ********************************************************************************
                                                     2893 *        Register equates
                                                     2894 ********************************************************************************

                                00000000  00000001  2896 R0       EQU   0
                                00000001  00000001  2897 R1       EQU   1
                                00000002  00000001  2898 R2       EQU   2
                                00000003  00000001  2899 R3       EQU   3
                                00000004  00000001  2900 R4       EQU   4
                                00000005  00000001  2901 R5       EQU   5
                                00000006  00000001  2902 R6       EQU   6
                                00000007  00000001  2903 R7       EQU   7
                                00000008  00000001  2904 R8       EQU   8
                                00000009  00000001  2905 R9       EQU   9
                                0000000A  00000001  2906 R10      EQU   10
                                0000000B  00000001  2907 R11      EQU   11
                                0000000C  00000001  2908 R12      EQU   12
                                0000000D  00000001  2909 R13      EQU   13
                                0000000E  00000001  2910 R14      EQU   14
                                0000000F  00000001  2911 R15      EQU   15

                                                     2913 ********************************************************************************
                                                     2914 *        Register equates
                                                     2915 ********************************************************************************

                                00000000  00000001  2917 FPR0     EQU   0
                                00000001  00000001  2918 FPR1     EQU   1
                                00000002  00000001  2919 FPR2     EQU   2
                                00000003  00000001  2920 FPR3     EQU   3
                                00000004  00000001  2921 FPR4     EQU   4
                                00000005  00000001  2922 FPR5     EQU   5
                                00000006  00000001  2923 FPR6     EQU   6
                                00000007  00000001  2924 FPR7     EQU   7
                                00000008  00000001  2925 FPR8     EQU   8
                                00000009  00000001  2926 FPR9     EQU   9
                                0000000A  00000001  2927 FPR10    EQU   10
                                0000000B  00000001  2928 FPR11    EQU   11
                                0000000C  00000001  2929 FPR12    EQU   12
                                0000000D  00000001  2930 FPR13    EQU   13
                                0000000E  00000001  2931 FPR14    EQU   14
                                0000000F  00000001  2932 FPR15    EQU   15

                                                     2934 ********************************************************************************
                                                     2935 *        Register equates
                                                     2936 ********************************************************************************

                                00000000  00000001  2938 V0       EQU   0
                                00000001  00000001  2939 V1       EQU   1
                                00000002  00000001  2940 V2       EQU   2
                                00000003  00000001  2941 V3       EQU   3
                                00000004  00000001  2942 V4       EQU   4
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2    STMT
                                00000005  00000001  2943 V5       EQU   5
                                00000006  00000001  2944 V6       EQU   6
                                00000007  00000001  2945 V7       EQU   7
                                00000008  00000001  2946 V8       EQU   8
                                00000009  00000001  2947 V9       EQU   9
                                0000000A  00000001  2948 V10      EQU   10
                                0000000B  00000001  2949 V11      EQU   11
                                0000000C  00000001  2950 V12      EQU   12
                                0000000D  00000001  2951 V13      EQU   13
                                0000000E  00000001  2952 V14      EQU   14
                                0000000F  00000001  2953 V15      EQU   15
                                00000010  00000001  2954 V16      EQU   16
                                00000011  00000001  2955 V17      EQU   17
                                00000012  00000001  2956 V18      EQU   18
                                00000013  00000001  2957 V19      EQU   19
                                00000014  00000001  2958 V20      EQU   20
                                00000015  00000001  2959 V21      EQU   21
                                00000016  00000001  2960 V22      EQU   22
                                00000017  00000001  2961 V23      EQU   23
                                00000018  00000001  2962 V24      EQU   24
                                00000019  00000001  2963 V25      EQU   25
                                0000001A  00000001  2964 V26      EQU   26
                                0000001B  00000001  2965 V27      EQU   27
                                0000001C  00000001  2966 V28      EQU   28
                                0000001D  00000001  2967 V29      EQU   29
                                0000001E  00000001  2968 V30      EQU   30
                                0000001F  00000001  2969 V31      EQU   31
                                                    2970
                                                    2971          END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
BEGIN	I	00000200	2	176	141 172 173 174
CTLR0	F	000006BC	4	542	186 187 188 189
DECNUM	C	000010CA	16	627	373 375 382 384 389 391 418 420 427 429 434 436
DONEXT	U	0000033E	1	264	258
E6TEST	4	00000000	144	641	235
E6TESTS	F	000038CC	4	2835	228
EDIT	X	0000109E	18	622	374 383 390 419 428 435
ENDTEST	U	00000590	1	456	233
EOJ	I	000006A0	4	532	221 459
EOJPSW	D	00000690	8	530	532
FAILCONT	U	00000580	1	446	
FAILED	F	00001000	4	581	401 448 457
FAILMSG	U	00000518	1	416	248 250 262
FAILPSW	D	000006A8	8	534	536
FAILTEST	I	000006B8	4	536	460
FB0001	F	00000298	8	205	209 210 212
FLG	X	0000000A	1	648	247
FLG1	X	0000112A	1	796	
FLG10	X	000018C2	1	1183	
FLG11	X	0000199A	1	1226	
FLG12	X	00001A72	1	1269	
FLG13	X	00001B4A	1	1318	
FLG14	X	00001C22	1	1361	
FLG15	X	00001CFA	1	1404	
FLG16	X	00001DD2	1	1447	
FLG17	X	00001EAA	1	1490	
FLG18	X	00001F82	1	1533	
FLG19	X	0000205A	1	1577	
FLG2	X	00001202	1	839	
FLG20	X	00002132	1	1620	
FLG21	X	0000220A	1	1663	
FLG22	X	000022E2	1	1706	
FLG23	X	000023BA	1	1749	
FLG24	X	00002492	1	1798	
FLG25	X	0000256A	1	1841	
FLG26	X	00002642	1	1884	
FLG27	X	0000271A	1	1927	
FLG28	X	000027F2	1	1970	
FLG29	X	000028CA	1	2013	
FLG3	X	000012DA	1	881	
FLG30	X	000029A2	1	2056	
FLG31	X	00002A7A	1	2100	
FLG32	X	00002B52	1	2144	
FLG33	X	00002C2A	1	2187	
FLG34	X	00002D02	1	2230	
FLG35	X	00002DDA	1	2273	
FLG36	X	00002EB2	1	2316	
FLG37	X	00002F8A	1	2365	
FLG38	X	00003062	1	2408	
FLG39	X	0000313A	1	2451	
FLG4	X	000013B2	1	924	
FLG40	X	00003212	1	2494	
FLG41	X	000032EA	1	2537	
FLG42	X	000033C2	1	2580	
FLG43	X	0000349A	1	2624	
FLG44	X	00003572	1	2667	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
FLG45	X	0000364A	1	2710	
FLG46	X	00003722	1	2753	
FLG47	X	000037FA	1	2796	
FLG5	X	0000148A	1	967	
FLG6	X	00001562	1	1010	
FLG7	X	0000163A	1	1053	
FLG8	X	00001712	1	1097	
FLG9	X	000017EA	1	1140	
FPCINIT	X	000006C4	4	544	300 318 336 354 817 860 902 945 988 1031 1074 1118 1161 1204 1247 1290 1339 1382 1425 1468 1511 1554 1598 1641 1684 1727 1770 1819 1862 1905 1948 1991 2034 2077 2121 2165 2208 2251 2294 2337 2386 2429 2472 2515 2558 2601 2645 2688 2731 2774 2817
FPC_R	F	00000040	4	657	247 249 255 276
FPC_R_1	F	00001160	4	805	821
FPC_R_10	F	000018F8	4	1192	1208
FPC_R_11	F	000019D0	4	1235	1251
FPC_R_12	F	00001AA8	4	1278	1294
FPC_R_13	F	00001B80	4	1327	1343
FPC_R_14	F	00001C58	4	1370	1386
FPC_R_15	F	00001D30	4	1413	1429
FPC_R_16	F	00001E08	4	1456	1472
FPC_R_17	F	00001EE0	4	1499	1515
FPC_R_18	F	00001FB8	4	1542	1558
FPC_R_19	F	00002090	4	1586	1602
FPC_R_2	F	00001238	4	848	864
FPC_R_20	F	00002168	4	1629	1645
FPC_R_21	F	00002240	4	1672	1688
FPC_R_22	F	00002318	4	1715	1731
FPC_R_23	F	000023F0	4	1758	1774
FPC_R_24	F	000024C8	4	1807	1823
FPC_R_25	F	000025A0	4	1850	1866
FPC_R_26	F	00002678	4	1893	1909
FPC_R_27	F	00002750	4	1936	1952
FPC_R_28	F	00002828	4	1979	1995
FPC_R_29	F	00002900	4	2022	2038
FPC_R_3	F	00001310	4	890	906
FPC_R_30	F	000029D8	4	2065	2081
FPC_R_31	F	00002AB0	4	2109	2125
FPC_R_32	F	00002B88	4	2153	2169
FPC_R_33	F	00002C60	4	2196	2212
FPC_R_34	F	00002D38	4	2239	2255
FPC_R_35	F	00002E10	4	2282	2298
FPC_R_36	F	00002EE8	4	2325	2341
FPC_R_37	F	00002FC0	4	2374	2390
FPC_R_38	F	00003098	4	2417	2433
FPC_R_39	F	00003170	4	2460	2476
FPC_R_4	F	000013E8	4	933	949
FPC_R_40	F	00003248	4	2503	2519
FPC_R_41	F	00003320	4	2546	2562
FPC_R_42	F	000033F8	4	2589	2605
FPC_R_43	F	000034D0	4	2633	2649
FPC_R_44	F	000035A8	4	2676	2692
FPC_R_45	F	00003680	4	2719	2735
FPC_R_46	F	00003758	4	2762	2778
FPC_R_47	F	00003830	4	2805	2821
FPC_R_5	F	000014C0	4	976	992

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
FPC_R_6	F	00001598	4	1019	1035
FPC_R_7	F	00001670	4	1062	1078
FPC_R_8	F	00001748	4	1106	1122
FPC_R_9	F	00001820	4	1149	1165
FPC_XC	F	00000078	4	663	304 307 322 325 340 343 358 361
FPC_XC_1	F	00001198	4	811	
FPC_XC_10	F	00001930	4	1198	
FPC_XC_11	F	00001A08	4	1241	
FPC_XC_12	F	00001AE0	4	1284	
FPC_XC_13	F	00001BB8	4	1333	
FPC_XC_14	F	00001C90	4	1376	
FPC_XC_15	F	00001D68	4	1419	
FPC_XC_16	F	00001E40	4	1462	
FPC_XC_17	F	00001F18	4	1505	
FPC_XC_18	F	00001FF0	4	1548	
FPC_XC_19	F	000020C8	4	1592	
FPC_XC_2	F	00001270	4	854	
FPC_XC_20	F	000021A0	4	1635	
FPC_XC_21	F	00002278	4	1678	
FPC_XC_22	F	00002350	4	1721	
FPC_XC_23	F	00002428	4	1764	
FPC_XC_24	F	00002500	4	1813	
FPC_XC_25	F	000025D8	4	1856	
FPC_XC_26	F	000026B0	4	1899	
FPC_XC_27	F	00002788	4	1942	
FPC_XC_28	F	00002860	4	1985	
FPC_XC_29	F	00002938	4	2028	
FPC_XC_3	F	00001348	4	896	
FPC_XC_30	F	00002A10	4	2071	
FPC_XC_31	F	00002AE8	4	2115	
FPC_XC_32	F	00002BC0	4	2159	
FPC_XC_33	F	00002C98	4	2202	
FPC_XC_34	F	00002D70	4	2245	
FPC_XC_35	F	00002E48	4	2288	
FPC_XC_36	F	00002F20	4	2331	
FPC_XC_37	F	00002FF8	4	2380	
FPC_XC_38	F	000030D0	4	2423	
FPC_XC_39	F	000031A8	4	2466	
FPC_XC_4	F	00001420	4	939	
FPC_XC_40	F	00003280	4	2509	
FPC_XC_41	F	00003358	4	2552	
FPC_XC_42	F	00003430	4	2595	
FPC_XC_43	F	00003508	4	2639	
FPC_XC_44	F	000035E0	4	2682	
FPC_XC_45	F	000036B8	4	2725	
FPC_XC_46	F	00003790	4	2768	
FPC_XC_47	F	00003868	4	2811	
FPC_XC_5	F	000014F8	4	982	
FPC_XC_6	F	000015D0	4	1025	
FPC_XC_7	F	000016A8	4	1068	
FPC_XC_8	F	00001780	4	1112	
FPC_XC_9	F	00001858	4	1155	
FPR0	U	00000000	1	2917	
FPR1	U	00000001	1	2918	
FPR10	U	0000000A	1	2927	
FPR11	U	0000000B	1	2928	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
FPR12	U	0000000C	1	2929	
FPR13	U	0000000D	1	2930	
FPR14	U	0000000E	1	2931	
FPR15	U	0000000F	1	2932	
FPR2	U	00000002	1	2919	
FPR3	U	00000003	1	2920	
FPR4	U	00000004	1	2921	
FPR5	U	00000005	1	2922	
FPR6	U	00000006	1	2923	
FPR7	U	00000007	1	2924	
FPR8	U	00000008	1	2925	
FPR9	U	00000009	1	2926	
IMAGE	1	00000000	14744	0	
K	U	00000400	1	564	565 566 567
K64	U	00010000	1	566	
M3	U	00000008	1	646	381 426
M4	U	00000009	1	647	388 433
MB	U	00100000	1	567	
MSG	I	000005D8	4	492	220 475
MSGCMD	C	00000626	9	522	505 506
MSGMSG	C	0000062F	95	523	499 520 497
MSGMVC	I	00000620	6	520	503
MSGOK	I	000005EE	2	501	498
MSGRET	I	0000060E	4	516	509 512
MSGSAVE	F	00000614	4	519	495 516
NEXTE6	U	000002EC	1	230	266 451
OPNAME	C	00000010	8	651	282 285 288 291 378 423
PAGE	U	00001000	1	565	
PRT3	C	000010B4	18	625	374 375 376 383 384 385 390 391 392 419 420 421 428 429 430 435 436 437
PRTLINE	C	00001008	13	590	600 440
PRTLNG	U	00000048	1	600	439
PRTM3	C	00001041	2	595	430
PRTM4	C	0000104D	2	598	437
PRTNAME	C	00001030	8	593	423
PRTNUM	C	00001015	3	591	421
R0	U	00000000	1	2896	135 186 189 209 211 212 213 218 237 238 395 400 401 439 447 448 474 476 492 495 497 499 501 516
R1	U	00000001	1	2897	219 254 255 256 257 260 261 310 311 328 329 346 347 364 365 396 440 457 458 506 520
R10	U	0000000A	1	2906	174 183 184
R11	U	0000000B	1	2907	240 241 823 866 908 951 994 1037 1080 1124 1167 1210 1253 1296 1345 1388 1431 1474 1517 1560 1604 1647 1690 1733 1776 1825 1868 1911 1954 1997 2040 2083 2127 2171 2214 2257 2300 2343 2392 2435 2478 2521 2564 2607 2651 2694 2737 2780 2823
R12	U	0000000C	1	2908	228 231 265 450
R13	U	0000000D	1	2909	
R14	U	0000000E	1	2910	
R15	U	0000000F	1	2911	243 275 277 295 308 313 326 331 344 349 362 367 394 397 398 402 441 469 479 480
R2	U	00000002	1	2898	220 372 373 380 381 382 387 388 389 417 418 425 426 427 432 433 434 474 475 476 493 495 501 502 503 505 511 516 517 818 819 861 862 903 904 946 947 989 990 1032 1033 1075 1076 1119 1120 1162 1163 1205 1206 1248 1249 1291 1292 1340 1341 1383 1384 1426 1427 1469 1470 1512 1513 1555 1556 1599 1600 1642 1643 1685 1686 1728 1729 1771 1772 1820 1821 1863

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					1864 1906 1907 1949 1950 1992 1993 2035 2036 2078 2079 2122 2123
					2166 2167 2209 2210 2252 2253 2295 2296 2338 2339 2387 2388 2430
					2431 2473 2474 2516 2517 2559 2560 2602 2603 2646 2647 2689 2690
					2732 2733 2775 2776 2818 2819
R3	U	00000003	1	2899	
R4	U	00000004	1	2900	
R5	U	00000005	1	2901	231 232 235 470 478 789 825 832 868 874 910 917 953
					960 996 1003 1039 1046 1082 1090 1126 1133 1169 1176 1212 1219
					1255 1262 1298 1311 1347 1354 1390 1397 1433 1440 1476 1483 1519
					1526 1562 1570 1606 1613 1649 1656 1692 1699 1735 1742 1778 1791
					1827 1834 1870 1877 1913 1920 1956 1963 1999 2006 2042 2049 2085
					2093 2129 2137 2173 2180 2216 2223 2259 2266 2302 2309 2345 2358
					2394 2401 2437 2444 2480 2487 2523 2530 2566 2573 2609 2617 2653
					2660 2696 2703 2739 2746 2782 2789 2825
R6	U	00000006	1	2902	
R7	U	00000007	1	2903	
R8	U	00000008	1	2904	172 176 177 178 180
R9	U	00000009	1	2905	173 180 181 183
RE1	F	000011D4	4	824	798 801
RE10	F	0000196C	4	1211	1185 1188
RE11	F	00001A44	4	1254	1228 1231
RE12	F	00001B1C	4	1297	1271 1274
RE13	F	00001BF4	4	1346	1320 1323
RE14	F	00001CCC	4	1389	1363 1366
RE15	F	00001DA4	4	1432	1406 1409
RE16	F	00001E7C	4	1475	1449 1452
RE17	F	00001F54	4	1518	1492 1495
RE18	F	0000202C	4	1561	1535 1538
RE19	F	00002104	4	1605	1579 1582
RE2	F	000012AC	4	867	841 844
RE20	F	000021DC	4	1648	1622 1625
RE21	F	000022B4	4	1691	1665 1668
RE22	F	0000238C	4	1734	1708 1711
RE23	F	00002464	4	1777	1751 1754
RE24	F	0000253C	4	1826	1800 1803
RE25	F	00002614	4	1869	1843 1846
RE26	F	000026EC	4	1912	1886 1889
RE27	F	000027C4	4	1955	1929 1932
RE28	F	0000289C	4	1998	1972 1975
RE29	F	00002974	4	2041	2015 2018
RE3	F	00001384	4	909	883 886
RE30	F	00002A4C	4	2084	2058 2061
RE31	F	00002B24	4	2128	2102 2105
RE32	F	00002BFC	4	2172	2146 2149
RE33	F	00002CD4	4	2215	2189 2192
RE34	F	00002DAC	4	2258	2232 2235
RE35	F	00002E84	4	2301	2275 2278
RE36	F	00002F5C	4	2344	2318 2321
RE37	F	00003034	4	2393	2367 2370
RE38	F	0000310C	4	2436	2410 2413
RE39	F	000031E4	4	2479	2453 2456
RE4	F	0000145C	4	952	926 929
RE40	F	000032BC	4	2522	2496 2499
RE41	F	00003394	4	2565	2539 2542
RE42	F	0000346C	4	2608	2582 2585
RE43	F	00003544	4	2652	2626 2629

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES		
RE44	F	0000361C	4	2695	2669	2672	
RE45	F	000036F4	4	2738	2712	2715	
RE46	F	000037CC	4	2781	2755	2758	
RE47	F	000038A4	4	2824	2798	2801	
RE5	F	00001534	4	995	969	972	
RE6	F	0000160C	4	1038	1012	1015	
RE7	F	000016E4	4	1081	1055	1058	
RE8	F	000017BC	4	1125	1099	1102	
RE9	F	00001894	4	1168	1142	1145	
READDR	A	0000001C	4	653	260		
REG2LOW	U	000000DD	1	571			
REG2PATT	U	AABBCCDD	1	570			
RELEN	A	00000018	4	652			
RPTDWSAV	D	000005C8	8	485	474	476	
RPTERROR	I	0000059E	4	469	397	441	
RPTSAVE	F	000005BC	4	482	469	479	
RPTSVR5	F	000005C0	4	483	470	478	
SKIPXC	C	00000050	8	659	273	281	294
SKL0001	U	0000005F	1	202	218		
SKT0001	C	0000022A	26	199	202	219	
SVOLDPSW	U	00000140	0	137			
T1	A	00001120	4	790	2838		
T10	A	000018B8	4	1177	2847		
T11	A	00001990	4	1220	2848		
T12	A	00001A68	4	1263	2849		
T13	A	00001B40	4	1312	2850		
T14	A	00001C18	4	1355	2851		
T15	A	00001CF0	4	1398	2852		
T16	A	00001DC8	4	1441	2853		
T17	A	00001EA0	4	1484	2854		
T18	A	00001F78	4	1527	2855		
T19	A	00002050	4	1571	2856		
T2	A	000011F8	4	833	2839		
T20	A	00002128	4	1614	2857		
T21	A	00002200	4	1657	2858		
T22	A	000022D8	4	1700	2859		
T23	A	000023B0	4	1743	2860		
T24	A	00002488	4	1792	2861		
T25	A	00002560	4	1835	2862		
T26	A	00002638	4	1878	2863		
T27	A	00002710	4	1921	2864		
T28	A	000027E8	4	1964	2865		
T29	A	000028C0	4	2007	2866		
T3	A	000012D0	4	875	2840		
T30	A	00002998	4	2050	2867		
T31	A	00002A70	4	2094	2868		
T32	A	00002B48	4	2138	2869		
T33	A	00002C20	4	2181	2870		
T34	A	00002CF8	4	2224	2871		
T35	A	00002DD0	4	2267	2872		
T36	A	00002EA8	4	2310	2873		
T37	A	00002F80	4	2359	2874		
T38	A	00003058	4	2402	2875		
T39	A	00003130	4	2445	2876		
T4	A	000013A8	4	918	2841		
T40	A	00003208	4	2488	2877		

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T41	A	000032E0	4	2531	2878
T42	A	000033B8	4	2574	2879
T43	A	00003490	4	2618	2880
T44	A	00003568	4	2661	2881
T45	A	00003640	4	2704	2882
T46	A	00003718	4	2747	2883
T47	A	000037F0	4	2790	2884
T5	A	00001480	4	961	2842
T6	A	00001558	4	1004	2843
T7	A	00001630	4	1047	2844
T8	A	00001708	4	1091	2845
T9	A	000017E0	4	1134	2846
TESTING	F	00001004	4	582	238
TNUM	H	00000004	2	643	237 372 417
TSUB	A	00000000	4	642	240
TTABLE	F	000038CC	4	2837	
V0	U	00000000	1	2938	
V1	U	00000001	1	2939	
V10	U	0000000A	1	2948	
V11	U	0000000B	1	2949	
V12	U	0000000C	1	2950	
V13	U	0000000D	1	2951	
V14	U	0000000E	1	2952	
V15	U	0000000F	1	2953	303 305 321 323 339 341 357 359
V16	U	00000010	1	2954	302 303 320 321 338 339 356 357
V17	U	00000011	1	2955	
V18	U	00000012	1	2956	
V19	U	00000013	1	2957	
V1FUDGE	X	000010EA	16	633	
V1INPUT	X	000010FA	16	634	
V1O1	X	00001148	16	803	822
V1O10	X	000018E0	16	1190	1209
V1O11	X	000019B8	16	1233	1252
V1O12	X	00001A90	16	1276	1295
V1O13	X	00001B68	16	1325	1344
V1O14	X	00001C40	16	1368	1387
V1O15	X	00001D18	16	1411	1430
V1O16	X	00001DF0	16	1454	1473
V1O17	X	00001EC8	16	1497	1516
V1O18	X	00001FA0	16	1540	1559
V1O19	X	00002078	16	1584	1603
V1O2	X	00001220	16	846	865
V1O20	X	00002150	16	1627	1646
V1O21	X	00002228	16	1670	1689
V1O22	X	00002300	16	1713	1732
V1O23	X	000023D8	16	1756	1775
V1O24	X	000024B0	16	1805	1824
V1O25	X	00002588	16	1848	1867
V1O26	X	00002660	16	1891	1910
V1O27	X	00002738	16	1934	1953
V1O28	X	00002810	16	1977	1996
V1O29	X	000028E8	16	2020	2039
V1O3	X	000012F8	16	888	907
V1O30	X	000029C0	16	2063	2082
V1O31	X	00002A98	16	2107	2126
V1O32	X	00002B70	16	2151	2170

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1033	X	00002C48	16	2194	2213
V1034	X	00002D20	16	2237	2256
V1035	X	00002DF8	16	2280	2299
V1036	X	00002ED0	16	2323	2342
V1037	X	00002FA8	16	2372	2391
V1038	X	00003080	16	2415	2434
V1039	X	00003158	16	2458	2477
V104	X	000013D0	16	931	950
V1040	X	00003230	16	2501	2520
V1041	X	00003308	16	2544	2563
V1042	X	000033E0	16	2587	2606
V1043	X	000034B8	16	2631	2650
V1044	X	00003590	16	2674	2693
V1045	X	00003668	16	2717	2736
V1046	X	00003740	16	2760	2779
V1047	X	00003818	16	2803	2822
V105	X	000014A8	16	974	993
V106	X	00001580	16	1017	1036
V107	X	00001658	16	1060	1079
V108	X	00001730	16	1104	1123
V109	X	00001808	16	1147	1166
V1OUTPUT	X	00000028	16	655	261 302 320 338 356
V2	U	00000002	1	2940	
V20	U	00000014	1	2958	
V21	U	00000015	1	2959	
V22	U	00000016	1	2960	819 820 822 862 863 865 904 905 907 947 948 950 990 991 993 1033 1034 1036 1076 1077 1079 1120 1121 1123 1163 1164 1166 1206 1207 1209 1249 1250 1252 1292 1293 1295 1341 1342 1344 1384 1385 1387 1427 1428 1430 1470 1471 1473 1513 1514 1516 1556 1557 1559 1600 1601 1603 1643 1644 1646 1686 1687 1689 1729 1730 1732 1772 1773 1775 1821 1822 1824 1864 1865 1867 1907 1908 1910 1950 1951 1953 1993 1994 1996 2036 2037 2039 2079 2080 2082 2123 2124 2126 2167 2168 2170 2210 2211 2213 2253 2254 2256 2296 2297 2299 2339 2340 2342 2388 2389 2391 2431 2432 2434 2474 2475 2477 2517 2518 2520 2560 2561 2563 2603 2604 2606 2647 2648 2650 2690 2691 2693 2733 2734 2736 2776 2777 2779 2819 2820 2822
V23	U	00000017	1	2961	
V24	U	00000018	1	2962	
V25	U	00000019	1	2963	
V26	U	0000001A	1	2964	
V27	U	0000001B	1	2965	
V28	U	0000001C	1	2966	
V29	U	0000001D	1	2967	
V2ADDR	A	0000000C	4	650	310 328 346 364
V2_1	A	0000112C	4	798	818
V2_10	A	000018C4	4	1185	1205
V2_11	A	0000199C	4	1228	1248
V2_12	A	00001A74	4	1271	1291
V2_13	A	00001B4C	4	1320	1340
V2_14	A	00001C24	4	1363	1383
V2_15	A	00001CFC	4	1406	1426
V2_16	A	00001DD4	4	1449	1469
V2_17	A	00001EAC	4	1492	1512
V2_18	A	00001F84	4	1535	1555
V2_19	A	0000205C	4	1579	1599
V2_2	A	00001204	4	841	861

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V2_20	A	00002134	4	1622	1642
V2_21	A	0000220C	4	1665	1685
V2_22	A	000022E4	4	1708	1728
V2_23	A	000023BC	4	1751	1771
V2_24	A	00002494	4	1800	1820
V2_25	A	0000256C	4	1843	1863
V2_26	A	00002644	4	1886	1906
V2_27	A	0000271C	4	1929	1949
V2_28	A	000027F4	4	1972	1992
V2_29	A	000028CC	4	2015	2035
V2_3	A	000012DC	4	883	903
V2_30	A	000029A4	4	2058	2078
V2_31	A	00002A7C	4	2102	2122
V2_32	A	00002B54	4	2146	2166
V2_33	A	00002C2C	4	2189	2209
V2_34	A	00002D04	4	2232	2252
V2_35	A	00002DDC	4	2275	2295
V2_36	A	00002EB4	4	2318	2338
V2_37	A	00002F8C	4	2367	2387
V2_38	A	00003064	4	2410	2430
V2_39	A	0000313C	4	2453	2473
V2_4	A	000013B4	4	926	946
V2_40	A	00003214	4	2496	2516
V2_41	A	000032EC	4	2539	2559
V2_42	A	000033C4	4	2582	2602
V2_43	A	0000349C	4	2626	2646
V2_44	A	00003574	4	2669	2689
V2_45	A	0000364C	4	2712	2732
V2_46	A	00003724	4	2755	2775
V2_47	A	000037FC	4	2798	2818
V2_5	A	0000148C	4	969	989
V2_6	A	00001564	4	1012	1032
V2_7	A	0000163C	4	1055	1075
V2_8	A	00001714	4	1099	1119
V2_9	A	000017EC	4	1142	1162
V3	U	00000003	1	2941	
V30	U	0000001E	1	2968	
V31	U	0000001F	1	2969	
V4	U	00000004	1	2942	
V5	U	00000005	1	2943	
V6	U	00000006	1	2944	
V7	U	00000007	1	2945	
V8	U	00000008	1	2946	
V9	U	00000009	1	2947	
VXC	X	0000000B	1	649	249
VXC1	X	0000112B	1	797	
VXC10	X	000018C3	1	1184	
VXC11	X	0000199B	1	1227	
VXC12	X	00001A73	1	1270	
VXC13	X	00001B4B	1	1319	
VXC14	X	00001C23	1	1362	
VXC15	X	00001CFB	1	1405	
VXC16	X	00001DD3	1	1448	
VXC17	X	00001EAB	1	1491	
VXC18	X	00001F83	1	1534	
VXC19	X	0000205B	1	1578	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
VXC2	X	00001203	1	840	
VXC20	X	00002133	1	1621	
VXC21	X	0000220B	1	1664	
VXC22	X	000022E3	1	1707	
VXC23	X	000023BB	1	1750	
VXC24	X	00002493	1	1799	
VXC25	X	0000256B	1	1842	
VXC26	X	00002643	1	1885	
VXC27	X	0000271B	1	1928	
VXC28	X	000027F3	1	1971	
VXC29	X	000028CB	1	2014	
VXC3	X	000012DB	1	882	
VXC30	X	000029A3	1	2057	
VXC31	X	00002A7B	1	2101	
VXC32	X	00002B53	1	2145	
VXC33	X	00002C2B	1	2188	
VXC34	X	00002D03	1	2231	
VXC35	X	00002DDB	1	2274	
VXC36	X	00002EB3	1	2317	
VXC37	X	00002F8B	1	2366	
VXC38	X	00003063	1	2409	
VXC39	X	0000313B	1	2452	
VXC4	X	000013B3	1	925	
VXC40	X	00003213	1	2495	
VXC41	X	000032EB	1	2538	
VXC42	X	000033C3	1	2581	
VXC43	X	0000349B	1	2625	
VXC44	X	00003573	1	2668	
VXC45	X	0000364B	1	2711	
VXC46	X	00003723	1	2754	
VXC47	X	000037FB	1	2797	
VXC5	X	0000148B	1	968	
VXC6	X	00001563	1	1011	
VXC7	X	0000163B	1	1054	
VXC8	X	00001713	1	1098	
VXC9	X	000017EB	1	1141	
WK1	F	00000088	4	665	
WK2	F	0000008C	4	666	
X0001	U	000002C0	1	208	196 209
X1	F	000011B0	4	816	790
X10	F	00001948	4	1203	1177
X11	F	00001A20	4	1246	1220
X12	F	00001AF8	4	1289	1263
X13	F	00001BD0	4	1338	1312
X14	F	00001CA8	4	1381	1355
X15	F	00001D80	4	1424	1398
X16	F	00001E58	4	1467	1441
X17	F	00001F30	4	1510	1484
X18	F	00002008	4	1553	1527
X19	F	000020E0	4	1597	1571
X2	F	00001288	4	859	833
X20	F	000021B8	4	1640	1614
X21	F	00002290	4	1683	1657
X22	F	00002368	4	1726	1700
X23	F	00002440	4	1769	1743
X24	F	00002518	4	1818	1792

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X25	F	000025F0	4	1861	1835
X26	F	000026C8	4	1904	1878
X27	F	000027A0	4	1947	1921
X28	F	00002878	4	1990	1964
X29	F	00002950	4	2033	2007
X3	F	00001360	4	901	875
X30	F	00002A28	4	2076	2050
X31	F	00002B00	4	2120	2094
X32	F	00002BD8	4	2164	2138
X33	F	00002CB0	4	2207	2181
X34	F	00002D88	4	2250	2224
X35	F	00002E60	4	2293	2267
X36	F	00002F38	4	2336	2310
X37	F	00003010	4	2385	2359
X38	F	000030E8	4	2428	2402
X39	F	000031C0	4	2471	2445
X4	F	00001438	4	944	918
X40	F	00003298	4	2514	2488
X41	F	00003370	4	2557	2531
X42	F	00003448	4	2600	2574
X43	F	00003520	4	2644	2618
X44	F	000035F8	4	2687	2661
X45	F	000036D0	4	2730	2704
X46	F	000037A8	4	2773	2747
X47	F	00003880	4	2816	2790
X5	F	00001510	4	987	961
X6	F	000015E8	4	1030	1004
X7	F	000016C0	4	1073	1047
X8	F	00001798	4	1117	1091
X9	F	00001870	4	1160	1134
XC0001	U	000002E8	1	222	214
XCFAILMSG	H	00000464	2	371	312 330 348 366
XCHECK	U	00000346	1	272	243
XCO1	X	00001180	16	809	
XCO10	X	00001918	16	1196	
XCO11	X	000019F0	16	1239	
XCO12	X	00001AC8	16	1282	
XCO13	X	00001BA0	16	1331	
XCO14	X	00001C78	16	1374	
XCO15	X	00001D50	16	1417	
XCO16	X	00001E28	16	1460	
XCO17	X	00001F00	16	1503	
XCO18	X	00001FD8	16	1546	
XCO19	X	000020B0	16	1590	
XCO2	X	00001258	16	852	
XCO20	X	00002188	16	1633	
XCO21	X	00002260	16	1676	
XCO22	X	00002338	16	1719	
XCO23	X	00002410	16	1762	
XCO24	X	000024E8	16	1811	
XCO25	X	000025C0	16	1854	
XCO26	X	00002698	16	1897	
XCO27	X	00002770	16	1940	
XCO28	X	00002848	16	1983	
XCO29	X	00002920	16	2026	
XCO3	X	00001330	16	894	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
XCO30	X	000029F8	16	2069	
XCO31	X	00002AD0	16	2113	
XCO32	X	00002BA8	16	2157	
XCO33	X	00002C80	16	2200	
XCO34	X	00002D58	16	2243	
XCO35	X	00002E30	16	2286	
XCO36	X	00002F08	16	2329	
XCO37	X	00002FE0	16	2378	
XCO38	X	000030B8	16	2421	
XCO39	X	00003190	16	2464	
XCO4	X	00001408	16	937	
XCO40	X	00003268	16	2507	
XCO41	X	00003340	16	2550	
XCO42	X	00003418	16	2593	
XCO43	X	000034F0	16	2637	
XCO44	X	000035C8	16	2680	
XCO45	X	000036A0	16	2723	
XCO46	X	00003778	16	2766	
XCO47	X	00003850	16	2809	
XCO5	X	000014E0	16	980	
XCO6	X	000015B8	16	1023	
XCO7	X	00001690	16	1066	
XCO8	X	00001768	16	1110	
XCO9	X	00001840	16	1153	
XCOUTPUT	X	00000060	16	661	305 311 323 329 341 347 359 365
XCPLINE	C	00001050	13	608	617 396
XCPLNG	U	0000004E	1	617	395
XCPM3	C	00001090	2	613	385
XCPM4	C	0000109B	2	615	392
XCPNAME	C	0000107F	8	611	378
XCPTNUM	C	0000105D	3	609	376
XCR15	F	00000510	8	408	394 398
XCRESULT	X	000004E0	16	405	
XCSKIP	C	00000007	1	645	274
XCV1	X	000004F0	16	406	
XCV2	X	00000500	16	407	
XCVCFN	F	000003FC	4	335	289
XCVCLFNH	F	000003C8	4	317	286
XCVCLFNL	F	00000430	4	353	292
XCVCNF	F	00000394	4	299	283
ZVE6TST	J	00000000	14744	134	137 139 143 147 580 135
=A(E6TESTS)	A	000006FC	4	555	228
=AL2(L'MSGMSG)	R	0000070A	2	559	497
=CL1'S'	C	0000070C	1	560	274
=CL8' '	C	000006D0	8	549	281
=CL8'SKIP XC '	C	000006C8	8	548	273 294
=CL8'VCFN'	C	000006E8	8	552	288
=CL8'VCLFNH'	C	000006E0	8	551	285
=CL8'VCLFNL'	C	000006F0	8	553	291
=CL8'VCNF'	C	000006D8	8	550	282
=F'1'	F	00000704	4	557	400 447
=F'4'	F	000006F8	4	554	213
=H'0'	H	00000708	2	558	492
=XL4'00000008'	X	00000700	4	556	256

```
 MACRO    DEFN   REFERENCES

FCHECK     86    195
PTTABLE   744   2836
VRR_A     682    787    830    872    915    958   1001   1044   1088   1131   1174   1217   1260   1309   1352   1395   1438   1481
                1524   1568   1611   1654   1697   1740   1789   1832   1875   1918   1961   2004   2047   2091   2135   2178   2221
                2264   2307   2356   2399   2442   2485   2528   2571   2615   2658   2701   2744   2787
```

```
   DESC      SYMBOL    SIZE      POS         ADDR

Entry: 0

Image       IMAGE     14744  0000-3997  0000-3997
  Region              14744  0000-3997  0000-3997
    CSECT   ZVE6TST   14744  0000-3997  0000-3997
```

```
   STMT                          FILE NAME
1     /home/tn529/sharedvfp/tests/zvector-e6-20-NNPconvert.asm

** NO ERRORS FOUND **
```