```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                        2 ************************************************************************
                                                        3 *
                                                        4 *   Zvector E7 instruction tests for VRR-d encoded:
                                                        5 *
                                                        6 *   E7BC VGFMA  - VECTOR GALOIS FIELD MULTIPLY SUM AND ACCUMULATE
                                                        7 *
                                                        8 *        James Wekel July 2024
                                                        9 ************************************************************************


                                                       11 ************************************************************************
                                                       12 *
                                                       13 *        basic instruction tests
                                                       14 *
                                                       15 ************************************************************************
                                                       16 *  This program tests proper functioning of the z/arch E7 VRR-d
                                                       17 *  VECTOR GALOIS FIELD MULTIPLY SUM AND ACCUMULATE instruction.
                                                       18 *  Exceptions are not tested.
                                                       19 *
                                                       20 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                       21 *  obvious coding errors.  None of the tests are thorough.  They are
                                                       22 *  NOT designed to test all aspects of any of the instructions.
                                                       23 *
                                                       24 ************************************************************************
                                                       25 *
                                                       26 *   *Testcase zvector-e7-03-VGFMA: VECTOR E7 VRR-d instructions
                                                       27 *   *
                                                       28 *   *   Zvector E7 instruction tests for VRR-d encoded:
                                                       29 *   *
                                                       30 *   *   E7BC VGFMA  - VECTOR GALOIS FIELD MULTIPLY SUM AND ACCUMULATE
                                                       31 *   *
                                                       32 *   *   # ------------------------------------------------------------
                                                       33 *   *   #  This tests only the basic function of the instruction.
                                                       34 *   *   #  Exceptions are NOT tested.
                                                       35 *   *   # ------------------------------------------------------------
                                                       36 *   *
                                                       37 *   mainsize    2
                                                       38 *   numcpu      1
                                                       39 *   sysclear
                                                       40 *   archlvl     z/Arch
                                                       41 *
                                                       42 *   loadcore    "$(testpath)/zvector-e7-03-VGFMA.core" 0x0
                                                       43 *
                                                       44 *   diag8cmd    enable    # (needed for messages to Hercules console)
                                                       45 *   runtest     2
                                                       46 *   diag8cmd    disable   # (reset back to default)
                                                       47 *
                                                       48 *   *Done
                                                       49 *
                                                       50 ************************************************************************
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                      52 ************************************************************************
                                                      53 *        FCHECK Macro - Is a Facility Bit set?
                                                      54 *
                                                      55 *        If the facility bit is NOT set, an message is issued and
                                                      56 *        the test is skipped.
                                                      57 *
                                                      58 *        Fcheck uses R0, R1 and R2
                                                      59 *
                                                      60 * eg.    FCHECK 134,'vector-packed-decimal'
                                                      61 ************************************************************************
                                                      62          MACRO
                                                      63          FCHECK &BITNO,&NOTSETMSG
                                                      64 .*                      &BITNO : facility bit number to check
                                                      65 .*                      &NOTSETMSG : 'facility name'
                                                      66          LCLA  &FBBYTE           Facility bit in Byte
                                                      67          LCLA  &FBBIT            Facility bit within Byte
                                                      68
                                                      69          LCLA  &L(8)
                                                      70 &L(1)    SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                                      71
                                                      72 &FBBYTE  SETA  &BITNO/8
                                                      73 &FBBIT   SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                                      74 .*       MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                                      75
                                                      76          B     X&SYSNDX
                                                      77 *                                       Fcheck data area
                                                      78 *                                       skip messgae
                                                      79 SKT&SYSNDX DC  C'    Skipping tests: '
                                                      80          DC    C&NOTSETMSG
                                                      81          DC    C' (bit &BITNO) is not installed.'
                                                      82 SKL&SYSNDX EQU *-SKT&SYSNDX
                                                      83 *                                       facility bits
                                                      84          DS    FD                       gap
                                                      85 FB&SYSNDX DS   4FD
                                                      86          DS    FD                       gap
                                                      87 *
                                                      88 X&SYSNDX EQU *
                                                      89          LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                                      90          STFLE FB&SYSNDX                get facility bits
                                                      91
                                                      92          XGR   R0,R0
                                                      93          IC    R0,FB&SYSNDX+&FBBYTE     get fbit byte
                                                      94          N     R0,=F'&FBBIT'            is bit set?
                                                      95          BNZ   XC&SYSNDX
                                                      96 *
                                                      97 * facility bit not set, issue message and exit
                                                      98 *
                                                      99          LA    R0,SKL&SYSNDX            message length
                                                     100          LA    R1,SKT&SYSNDX            message address
                                                     101          BAL   R2,MSG
                                                     102
                                                     103          B     EOJ
                                                     104 XC&SYSNDX EQU *
                                                     105          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     107 ************************************************************************
                                                     108 *        Low core PSWs
                                                     109 ************************************************************************
                               00000000  00001D0B    110 ZVE7TST  START 0
00000000                       00000000              111          USING ZVE7TST,R0            Low core addressability
                                                     112
                               00000140  00000000    113 SVOLDPSW EQU   ZVE7TST+X'140'        z/Arch Supervisor call old PSW

00000000                       00000000  000001A0    115          ORG   ZVE7TST+X'1A0'       z/Architecure RESTART PSW
000001A0  00000001 80000000                        116          DC    X'0000000180000000'
000001A8  00000000 00000200                        117          DC    AD(BEGIN)

000001B0                       000001B0  000001D0    119          ORG   ZVE7TST+X'1D0'       z/Architecure PROGRAM CHECK PSW
000001D0  00020001 80000000                        120          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                        121          DC    AD(X'DEAD')

000001E0                       000001E0  00000200    123          ORG   ZVE7TST+X'200'       Start of actual test program...

                                                     125 ************************************************************************
                                                     126 *                The actual "ZVE7TST" program itself...
                                                     127 ************************************************************************
                                                     128 *
                                                     129 *  Architecture Mode: z/Arch
                                                     130 *  Register Usage:
                                                     131 *
                                                     132 *    R0       (work)
                                                     133 *    R1-4     (work)
                                                     134 *    R5       Testing control table - current test base
                                                     135 *    R6-R7    (work)
                                                     136 *    R8       First base register
                                                     137 *    R9       Second base register
                                                     138 *    R10      Third base register
                                                     139 *    R11      E7TEST call return
                                                     140 *    R12      E7TESTS register
                                                     141 *    R13      (work)
                                                     142 *    R14      Subroutine call
                                                     143 *    R15      Secondary Subroutine call or work
                                                     144 *
                                                     145 ************************************************************************

00000200                       00000200              147          USING  BEGIN,R8         FIRST Base Register
00000200                       00001200              148          USING  BEGIN+4096,R9    SECOND Base Register
00000200                       00002200              149          USING  BEGIN+8192,R10   THIRD Base Register

00000200  0580                                       151 BEGIN    BALR  R8,0              Initalize FIRST base register
00000202  0680                                       152          BCTR  R8,0              Initalize FIRST base register
00000204  0680                                       153          BCTR  R8,0              Initalize FIRST base register

00000206  4190 8800                    00000800      155          LA    R9,2048(,R8)      Initalize SECOND base register
0000020A  4190 9800                    00000800      156          LA    R9,2048(,R9)      Initalize SECOND base register
                                                     157
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

0000020E  41A0 9800                    00000800   158          LA    R10,2048(,R9)    Initalize THIRD base register
00000212  41A0 A800                    00000800   159          LA    R10,2048(,R10)   Initalize THIRD base register
                                                  160
00000216  B600 828C                    0000048C   161          STCTL R0,R0,CTLR0      Store CR0 to enable AFP
0000021A  9604 828D                    0000048D   162          OI    CTLR0+1,X'04'    Turn on AFP bit
0000021E  9602 828D                    0000048D   163          OI    CTLR0+1,X'02'    Turn on Vector bit
00000222  B700 828C                    0000048C   164          LCTL  R0,R0,CTLR0      Reload updated CR0
                                                  165
                                                  166 ********************************************************************
                                                  167 * Is Vector packed-decimal facility installed  (bit 134)
                                                  168 ********************************************************************
                                                  169
                                                  170          FCHECK 129,'z/Architecture vector facility'
00000226  47F0 80A8                    000002A8  171+         B     X0001
                                                  172+*                                  Fcheck data area
                                                  173+*                                  skip messgae
0000022A  40404040 E2928997                       174+SKT0001  DC    C'    Skipping tests: '
0000023E  A961C199 838889A3                       175+         DC    C'z/Architecture vector facility'
0000025C  404D8289 A340F1F2                       176+         DC    C' (bit 129) is not installed.'
                           0000004E    00000001   177+SKL0001  EQU   *-SKT0001
                                                  178+*                                  facility bits
00000278  00000000 00000000                       179+         DS    FD                 gap
00000280  00000000 00000000                       180+FB0001   DS    4FD
000002A0  00000000 00000000                       181+         DS    FD                 gap
                                                  182+*
                           000002A8    00000001   183+X0001    EQU   *
000002A8  4100 0004                    00000004   184+         LA    R0,((X0001-FB0001)/8)-1
000002AC  B2B0 8080                    00000280   185+         STFLE FB0001             get facility bits
000002B0  B982 0000                               186+         XGR   R0,R0
000002B4  4300 8090                    00000290   187+         IC    R0,FB0001+16       get fbit byte
000002B8  5400 8294                    00000494   188+         N     R0,=F'64'          is bit set?
000002BC  4770 80D0                    000002D0   189+         BNZ   XC0001
                                                  190+*
                                                  191+* facility bit not set, issue message and exit
                                                  192+*
000002C0  4100 004E                    0000004E   193+         LA    R0,SKL0001         message length
000002C4  4110 802A                    0000022A   194+         LA    R1,SKT0001         message address
000002C8  4520 81A8                    000003A8   195+         BAL   R2,MSG
000002CC  47F0 8270                    00000470   196+         B     EOJ
                           000002D0    00000001   197+XC0001    EQU   *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     199 ************************************************************************
                                                     200 *               Do tests in the E7TESTS table
                                                     201 ************************************************************************
                                                     202
000002D0  58C0 8298                         00000498  203          L     R12,=A(E7TESTS)       get table of test addresses
                                                     204
                                 000002D4   00000001  205 NEXTE6   EQU   *
000002D4  5850 C000                         00000000  206          L     R5,0(0,R12)       get test address
000002D8  1255                                        207          LTR   R5,R5                  have a test?
000002DA  4780 811E                         0000031E  208          BZ    ENDTEST                   done?
                                                     209
000002DE                         00000000           210          USING E7TEST,R5
                                                     211
000002DE  4800 5004                         00000004  212          LH    R0,TNUM             save current test number
000002E2  5000 8E04                         00001004  213          ST    R0,TESTING          for easy reference
                                                     214
000002E6  E710 8E94 0006                    00001094  215          VL    V1,V1FUDGE
000002EC  58B0 5000                         00000000  216          L     R11,TSUB            get address of test routine
000002F0  05BB                                        217          BALR  R11,R11             do test
                                                     218
000002F2  E310 5020 0014                    00000020  219          LGF   R1,READDR           get address of expected result
000002F8  D50F 5030 1000         00000030   00000000  220          CLC   V1OUTPUT,0(R1)      valid?
000002FE  4770 810A                         0000030A  221          BNE   FAILMSG                no, issue failed message
                                                     222
00000302  41C0 C004                         00000004  223          LA    R12,4(0,R12)        next test address
00000306  47F0 80D4                         000002D4  224          B     NEXTE6
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     226 ************************************************************************
                                                     227 * result not as expected:
                                                     228 *        issue message with test number, instruction under test
                                                     229 *              and instruction m4
                                                     230 ************************************************************************
                               0000030A  00000001    231 FAILMSG  EQU   *
0000030A  45F0 812C                      0000032C    232          BAL   R15,RPTERROR

                                                     234 ************************************************************************
                                                     235 * continue after a failed test
                                                     236 ************************************************************************
                               0000030E  00000001    237 FAILCONT EQU   *
0000030E  5800 829C                      0000049C    238          L     R0,=F'1'          set failed test indicator
00000312  5000 8E00                      00001000    239          ST    R0,FAILED
                                                     240
00000316  41C0 C004                      00000004    241          LA    R12,4(0,R12)      next test address
0000031A  47F0 80D4                      000002D4    242          B     NEXTE6


                                                     244 ************************************************************************
                                                     245 * end of testing; set ending psw
                                                     246 ************************************************************************
                               0000031E  00000001    247 ENDTEST  EQU   *
0000031E  5810 8E00                      00001000    248          L     R1,FAILED         did a test fail?
00000322  1211                                       249          LTR   R1,R1
00000324  4780 8270                      00000470    250          BZ    EOJ               No, exit
00000328  47F0 8288                      00000488    251          B     FAILTEST          Yes, exit with BAD PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    253 ********************************************************************************
                                                    254 *        RPTERROR                  Report instruction test in error
                                                    255 ********************************************************************************

0000032C  50F0 8190                          00000390   257 RPTERROR ST    R15,RPTSAVE          Save return address
00000330  5050 8194                          00000394   258          ST    R5,RPTSVR5           Save R5
                                                    259 *
00000334  4820 5004                          00000004   260          LH    R2,TNUM              get test number and convert
00000338  4E20 8E73                          00001073   261          CVD   R2,DECNUM
0000033C  D211 8E5D 8E47      0000105D       00001047   262          MVC   PRT3,EDIT
00000342  DE11 8E5D 8E73      0000105D       00001073   263          ED    PRT3,DECNUM
00000348  D202 8E18 8E6A      00001018       0000106A   264          MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                    265
0000034E  D207 8E33 5008      00001033       00000008   266          MVC   PRTNAME,OPNAME       fill in message with instruction
                                                    267 *
00000354  E320 5007 0076                     00000007   268          LB    R2,m5                get m5 and convert
0000035A  4E20 8E73                          00001073   269          CVD   R2,DECNUM
0000035E  D211 8E5D 8E47      0000105D       00001047   270          MVC   PRT3,EDIT
00000364  DE11 8E5D 8E73      0000105D       00001073   271          ED    PRT3,DECNUM
0000036A  D201 8E44 8E6B      00001044       0000106B   272          MVC   PRTM5(2),PRT3+14     fill in message with m4 field

                                                    274 *
                                                    275 *        Use Hercules Diagnose for Message to console
                                                    276 *
00000370  9002 8198                          00000398   277          STM   R0,R2,RPTDWSAV       save regs used by MSG
00000374  4100 003F                          0000003F   278          LA    R0,PRTLNG            message length
00000378  4110 8E08                          00001008   279          LA    R1,PRTLINE             messagfe address
0000037C  4520 81A8                          000003A8   280          BAL   R2,MSG               call Hercules console MSG display
00000380  9802 8198                          00000398   281          LM    R0,R2,RPTDWSAV       restore regs


00000384  5850 8194                          00000394   283          L     R5,RPTSVR5           Restore R5
00000388  58F0 8190                          00000390   284          L     R15,RPTSAVE          Restore return address
0000038C  07FF                               00000      285          BR    R15                  Return to caller

00000390  00000000                                 287 RPTSAVE  DC    F'0'                 R15 save area
00000394  00000000                                 288 RPTSVR5  DC    F'0'                 R5 save area

00000398  00000000 00000000                        290 RPTDWSAV DC    2D'0'                R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    292 ************************************************************************
                                                    293 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                    294 *              R2 = return address
                                                    295 ************************************************************************
000003A8  4900 82A0                    000004A0    297 MSG      CH    R0,=H'0'                Do we even HAVE a message?
000003AC  07D2                                     298          BNHR  R2                      No, ignore

000003AE  9002 81E4                    000003E4    300          STM   R0,R2,MSGSAVE           Save registers

000003B2  4900 82A2                    000004A2    302          CH    R0,=AL2(L'MSGMSG)       Message length within limits?
000003B6  47D0 81BE                    000003BE    303          BNH   MSGOK                   Yes, continue
000003BA  4100 005F                    0000005F    304          LA    R0,L'MSGMSG             No, set to maximum

000003BE  1820                                     306 MSGOK    LR    R2,R0                   Copy length to work register
000003C0  0620                                     307          BCTR  R2,0                    Minus-1 for execute
000003C2  4420 81F0                    000003F0    308          EX    R2,MSGMVC               Copy message to O/P buffer

000003C6  4120 200A                    0000000A    310          LA    R2,1+L'MSGCMD(,R2)      Calculate true command length
000003CA  4110 81F6                    000003F6    311          LA    R1,MSGCMD               Point to true command

000003CE  83120008                                 313          DC    X'83',X'12',X'0008'     Issue Hercules Diagnose X'008'
000003D2  4780 81DE                    000003DE    314          BZ    MSGRET                  Return if successful
                                                   315
000003D6  1222                                     316          LTR   R2,R2                   Is Diag8 Ry (R2) 0?
000003D8  4780 81DE                    000003DE    317          BZ    MSGRET                    an error occurred but coninue
                                                   318
000003DC  0000                                     319          DC    H'0'                    CRASH for debugging purposes

000003DE  9802 81E4                    000003E4    321 MSGRET   LM    R0,R2,MSGSAVE           Restore registers
000003E2  07F2                                     322          BR    R2                      Return to caller

000003E4  00000000 00000000                        324 MSGSAVE  DC    3F'0'                   Registers save area
000003F0  D200 81FF 1000      000003FF  00000000   325 MSGMVC   MVC   MSGMSG(0),0(R1)         Executed instruction

000003F6  D4E2C7D5 D6C8405C                        327 MSGCMD   DC    C'MSGNOH * '            *** HERCULES MESSAGE COMMAND ***
000003FF  40404040 40404040                        328 MSGMSG   DC    CL95' '                 The message text to be displayed
                                                   329
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                     331 ************************************************************************
                                                     332 *        Normal completion or Abnormal termination PSWs
                                                     333 ************************************************************************

00000460  00020001 80000000                          335 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)
00000470  B2B2 8260                    00000460      337 EOJ      LPSWE EOJPSW               Normal completion

00000478  00020001 80000000                          339 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')
00000488  B2B2 8278                    00000478      341 FAILTEST LPSWE FAILPSW              Abnormal termination

                                                     343 ************************************************************************
                                                     344 *        Working Storage
                                                     345 ************************************************************************

0000048C  00000000                                   347 CTLR0    DS    F                    CR0
00000490  00000000                                   348         DS    F

00000494                                             350         LTORG ,                    Literals pool
00000494  00000040                                   351               =F'64'
00000498  00001CBC                                   352               =A(E7TESTS)
0000049C  00000001                                   353               =F'1'
000004A0  0000                                       354               =H'0'
000004A2  005F                                       355               =AL2(L'MSGMSG)
                                                     356
                                                     357 *        some constants
                                                     358
                          00000400  00000001         359 K        EQU   1024               One KB
                          00001000  00000001         360 PAGE     EQU   (4*K)              Size of one page
                          00010000  00000001         361 K64      EQU   (64*K)             64 KB
                          00100000  00000001         362 MB       EQU   (K*K)               1 MB
                                                     363
                          AABBCCDD  00000001         364 REG2PATT EQU   X'AABBCCDD'     Polluted Register pattern
                          000000DD  00000001         365 REG2LOW  EQU         X'DD'     (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     367 *=====================================================================
                                                     368 *
                                                     369 *  NOTE: start data on an address that is easy to display
                                                     370 *        within Hercules
                                                     371 *
                                                     372 *=====================================================================
                                                     373
000004A4                      000004A4  00001000     374          ORG   ZVE7TST+X'1000'
00001000  00000000                                   375 FAILED   DC    F'0'                    some test failed?
00001004  00000000                                   376 TESTING  DC    F'0'                    current test number

                                                     378 *
                                                     379 *        failed message and associated editting
                                                     380 *
00001008  40404040 40404040                          381 PRTLINE  DC    C'         Test # '
00001018  A7A7A7                                     382 PRTNUM   DC    C'xxx'
0000101B  40868189 93858440                          383          DC    c' failed for instruction '
00001033  A7A7A7A7 A7A7A7A7                          384 PRTNAME  DC    CL8'xxxxxxxx'
0000103B  40A689A3 884094F5                          385          DC    C' with m5='
00001044  A7A7                                       386 PRTM5    DC    C'xx'
00001046  4B                                         387          DC    C'.'
                                0000003F  00000001   388 PRTLNG   EQU   *-PRTLINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    390 ************************************************************************
                                                    391 *        TEST failed : message working storge
                                                    392 ************************************************************************
00001047  40212020 20202020                         393 EDIT     DC    XL18'402120202020202020202020202020202020'
                                                    394
00001059  7E7E7E6E                                  395          DC    C'===>'
0000105D  40404040 40404040                         396 PRT3     DC    CL18' '
0000106F  4C7E7E7E                                  397          DC    C'<==='
00001073  00000000 00000000                         398 DECNUM   DS    CL16


                                                    400 ************************************************************************
                                                    401 *        Vector instruction results, pollution and input
                                                    402 ************************************************************************
00001084                                            403          DS    0F
00001084  00000000 00000000                         404          DS    XL16                                        gap
00001094  FFFFFFFF FFFFFFFF                         405 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
000010A4  00000000 00000000                         406          DS    XL16
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     408 ************************************************************************
                                                     409 *        E7TEST DSECT
                                                     410 ************************************************************************


                                                     412 E7TEST   DSECT ,
00000000  00000000                                   413 TSUB     DC    A(0)           pointer  to test
00000004  0000                                       414 TNUM     DC    H'00'          Test Number
00000006  00                                         415          DC    X'00'
00000007  00                                         416 M5       DC    HL1'00'        m4 used
                                                     417
00000008  40404040 40404040                          418 OPNAME   DC    CL8' '         E6 name
00000010  00000000                                   419 V2ADDR   DC    A(0)           address of v2 source
00000014  00000000                                   420 V3ADDR   DC    A(0)           address of v3 source
00000018  00000000                                   421 V4ADDR   DC    A(0)           address of v4 source
0000001C  00000000                                   422 RELEN    DC    A(0)           RESULT LENGTH
00000020  00000000                                   423 READDR   DC    A(0)           result (expected) address
00000028  00000000 00000000                          424          DS    FD                gap
00000030  00000000 00000000                          425 V1OUTPUT DS    XL16           V1 Output
00000040  00000000 00000000                          426          DS    FD                gap
                                                     427
                                                     428 *        test routine will be here (from VRR-d macro)
                                                     429 *
                                                     430 *        followed by
                                                     431 *              EXPECTED RESULT


                          00000000  00001D0B   433 ZVE7TST  CSECT ,
000010B4                                             434          DS    0F


                                                     436 ************************************************************************
                                                     437 *     Macros to help build test tables
                                                     438 ************************************************************************


                                                     440 *
                                                     441 * macro to generate individual test
                                                     442 *
                                                     443          MACRO
                                                     444          VRR_D &INST,&M5
                                                     445 .*                              &INST   - VRR-d instruction under test
                                                     446 .*                              &m5     - m3 field
                                                     447
                                                     448          GBLA  &TNUM
                                                     449 &TNUM    SETA  &TNUM+1
                                                     450
                                                     451          DS    0FD
                                                     452          USING *,R5             base for test data and test routine
                                                     453
                                                     454 T&TNUM   DC    A(X&TNUM)        address of test routine
                                                     455          DC    H'&TNUM'         test number
                                                     456          DC    X'00'
                                                     457          DC    HL1'&M5'         m5
                                                     458          DC    CL8'&INST'       instruction name
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                      459           DC    A(RE&TNUM+16)     address of v2 source
                                                      460           DC    A(RE&TNUM+32)     address of v3 source
                                                      461           DC    A(RE&TNUM+48)     address of v4 source
                                                      462           DC    A(16)             result length
                                                      463 REA&TNUM  DC    A(RE&TNUM)        result address
                                                      464           DS    FD                gap
                                                      465 V1O&TNUM  DS    XL16              V1 output
                                                      466           DS    FD                gap
                                                      467 .*
                                                      468 *
                                                      469 X&TNUM    DS    0F
                                                      470           LGF   R1,V2ADDR         load v2 source
                                                      471           VL    v22,0(R1)         use v22 to test decoder
                                                      472
                                                      473           LGF   R1,V3ADDR         load v3 source
                                                      474           VL    v23,0(R1)         use v23 to test decoder
                                                      475
                                                      476           LGF   R1,V4ADDR         load v4 source
                                                      477           VL    v24,0(R1)         use v24 to test decoder
                                                      478
                                                      479           &INST V22,V22,V23,V24,&M5  test instruction (dest is a source)
                                                      480           VST   V22,V1O&TNUM       save v1 output
                                                      481
                                                      482           BR    R11               return
                                                      483
                                                      484 RE&TNUM   DC    0F                xl16 expected result
                                                      485
                                                      486           DROP  R5
                                                      487           MEND



                                                      489 *
                                                      490 * macro to generate table of pointers to individual tests
                                                      491 *
                                                      492           MACRO
                                                      493           PTTABLE
                                                      494           GBLA  &TNUM
                                                      495           LCLA  &CUR
                                                      496 &CUR      SETA  1
                                                      497 .*
                                                      498 TTABLE    DS    0F
                                                      499 .LOOP     ANOP
                                                      500 .*
                                                      501           DC    A(T&CUR)          TEST &CUR
                                                      502 .*
                                                      503 &CUR      SETA  &CUR+1
                                                      504           AIF   (&CUR LE &TNUM).LOOP
                                                      505 *
                                                      506           DC    A(0)              END OF TABLE
                                                      507           DC    A(0)
                                                      508 .*
                                                      509           MEND
                                                      510
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   512 ************************************************************************
                                                   513 *        E7 VRR-d tests
                                                   514 ************************************************************************
                                                   515          PRINT DATA
                                                   516 *
                                                   517 *   EE7BC VGFMA  - VECTOR GALOIS FIELD MULTIPLY SUM AND ACCUMULATE
                                                   518 *
                                                   519 *        VRR-d instruction, m5
                                                   520 *              followed by
                                                   521 *                 16 byte expected result (V1)
                                                   522 *                 16 byte V2 source
                                                   523 *                 16 byte V3 source
                                                   524 *                 16 byte V4 source
                                                   525 *-----------------------------------------------------------------------
                                                   526 * VGFMA  - VECTOR GALOIS FIELD MULTIPLY SUM AND ACCUMULATE
                                                   527 *-----------------------------------------------------------------------
                                                   528
                                                   529 *-----------------------------------------------------------------------
                                                   530 * case 0 - simple, simple debug
                                                   531 *-----------------------------------------------------------------------
                                                   532 * Byte
                                                   533          VRR_D VGFMA,0
000010B8                                           534+         DS    0FD
000010B8                          000010B8         535+         USING *,R5              base for test data and test routine
000010B8  00001100                                 536+T1       DC    A(X1)             address of test routine
000010BC  0001                                     537+         DC    H'1'              test number
000010BE  00                                       538+         DC    X'00'
000010BF  00                                       539+         DC    HL1'0'            m5
000010C0  E5C7C6D4 C1404040                        540+         DC    CL8'VGFMA'        instruction name
000010C8  00001144                                 541+         DC    A(RE1+16)         address of v2 source
000010CC  00001154                                 542+         DC    A(RE1+32)         address of v3 source
000010D0  00001164                                 543+         DC    A(RE1+48)         address of v4 source
000010D4  00000010                                 544+         DC    A(16)             result length
000010D8  00001134                                 545+REA1     DC    A(RE1)            result address
000010E0  00000000 00000000                        546+         DS    FD                gap
000010E8  00000000 00000000                        547+V1O1     DS    XL16              V1 output
000010F0  00000000 00000000
000010F8  00000000 00000000                        548+         DS    FD                gap
                                                   549+*
00001100                                           550+X1       DS    0F
00001100  E310 5010 0014                 00000010  551+         LGF   R1,V2ADDR         load v2 source
00001106  E761 0000 0806                 00000000  552+         VL    v22,0(R1)         use v22 to test decoder
0000110C  E310 5014 0014                 00000014  553+         LGF   R1,V3ADDR         load v3 source
00001112  E771 0000 0806                 00000000  554+         VL    v23,0(R1)         use v23 to test decoder
00001118  E310 5018 0014                 00000018  555+         LGF   R1,V4ADDR         load v4 source
0000111E  E781 0000 0806                 00000000  556+         VL    v24,0(R1)         use v24 to test decoder
00001124  E766 7000 8FBC                           557+         VGFMA V22,V22,V23,V24,0    test instruction (dest is a source)
0000112A  E760 5030 080E                 000010E8  558+         VST   V22,V1O1           save v1 output
00001130  07FB                                     559+         BR    R11               return
00001134                                           560+RE1      DC    0F                xl16 expected result
00001134                                           561+         DROP  R5
00001134  01000080 00000000                        562          DC    XL16'01000080000000000000000000000000'   expected result
0000113C  00000000 00000000
00001144  80008080 00000000                        563          DC    XL16'80008080000000000000000000000000'   v2
0000114C  00000000 00000000
00001154  02000203 00000000                        564          DC    XL16'02000203000000000000000000000000'   v3
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

0000115C  00000000 00000000
00001164  00000000 00000000                        565          DC    XL16'00000000000000000000000000000000'   v4
0000116C  00000000 00000000
                                                   566
                                                   567 * Halfword
                                                   568          VRR_D VGFMA,1
00001178                                           569+         DS    0FD
00001178                      00001178             570+         USING *,R5              base for test data and test routine
00001178  000011C0                                 571+T2       DC    A(X2)             address of test routine
0000117C  0002                                     572+         DC    H'2'              test number
0000117E  00                                       573+         DC    X'00'
0000117F  01                                       574+         DC    HL1'1'            m5
00001180  E5C7C6D4 C1404040                        575+         DC    CL8'VGFMA'        instruction name
00001188  00001204                                 576+         DC    A(RE2+16)         address of v2 source
0000118C  00001214                                 577+         DC    A(RE2+32)         address of v3 source
00001190  00001224                                 578+         DC    A(RE2+48)         address of v4 source
00001194  00000010                                 579+         DC    A(16)             result length
00001198  000011F4                                 580+REA2     DC    A(RE2)            result address
000011A0  00000000 00000000                        581+         DS    FD                gap
000011A8  00000000 00000000                        582+V1O2     DS    XL16              V1 output
000011B0  00000000 00000000
000011B8  00000000 00000000                        583+         DS    FD                gap
                                                   584+*
000011C0                                           585+X2       DS    0F
000011C0  E310 5010 0014                00000010   586+         LGF   R1,V2ADDR         load v2 source
000011C6  E761 0000 0806                00000000   587+         VL    v22,0(R1)         use v22 to test decoder
000011CC  E310 5014 0014                00000014   588+         LGF   R1,V3ADDR         load v3 source
000011D2  E771 0000 0806                00000000   589+         VL    v23,0(R1)         use v23 to test decoder
000011D8  E310 5018 0014                00000018   590+         LGF   R1,V4ADDR         load v4 source
000011DE  E781 0000 0806                00000000   591+         VL    v24,0(R1)         use v24 to test decoder
000011E4  E766 7100 8FBC                           592+         VGFMA V22,V22,V23,V24,1    test instruction (dest is a source)
000011EA  E760 5030 080E                000011A8   593+         VST   V22,V1O2           save v1 output
000011F0  07FB                                     594+         BR    R11               return
000011F4                                           595+RE2      DC    0F                xl16 expected result
000011F4                                           596+         DROP  R5
000011F4  00010000 00000000                        597          DC    XL16'00010000000000000000000000000000'   expected result
000011FC  00000000 00000000
00001204  80000000 00000000                        598          DC    XL16'80000000000000000000000000000000'   v2
0000120C  00000000 00000000
00001214  00020000 00000000                        599          DC    XL16'00020000000000000000000000000000'   v3
0000121C  00000000 00000000
00001224  00000000 00000000                        600          DC    XL16'00000000000000000000000000000000'   v4
0000122C  00000000 00000000
                                                   601
                                                   602 * Word
                                                   603          VRR_D VGFMA,2
00001238                                           604+         DS    0FD
00001238                      00001238             605+         USING *,R5              base for test data and test routine
00001238  00001280                                 606+T3       DC    A(X3)             address of test routine
0000123C  0003                                     607+         DC    H'3'              test number
0000123E  00                                       608+         DC    X'00'
0000123F  02                                       609+         DC    HL1'2'            m5
00001240  E5C7C6D4 C1404040                        610+         DC    CL8'VGFMA'        instruction name
00001248  000012C4                                 611+         DC    A(RE3+16)         address of v2 source
0000124C  000012D4                                 612+         DC    A(RE3+32)         address of v3 source
00001250  000012E4                                 613+         DC    A(RE3+48)         address of v4 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
00001254  00000010                          614+         DC    A(16)             result length
00001258  000012B4                          615+REA3     DC    A(RE3)            result address
00001260  00000000 00000000                 616+         DS    FD                gap
00001268  00000000 00000000                 617+V1O3     DS    XL16              V1 output
00001270  00000000 00000000
00001278  00000000 00000000                 618+         DS    FD                gap
                                            619+*
00001280                                    620+X3       DS    0F
00001280  E310 5010 0014          00000010  621+         LGF   R1,V2ADDR         load v2 source
00001286  E761 0000 0806          00000000  622+         VL    v22,0(R1)         use v22 to test decoder
0000128C  E310 5014 0014          00000014  623+         LGF   R1,V3ADDR         load v3 source
00001292  E771 0000 0806          00000000  624+         VL    v23,0(R1)         use v23 to test decoder
00001298  E310 5018 0014          00000018  625+         LGF   R1,V4ADDR         load v4 source
0000129E  E781 0000 0806          00000000  626+         VL    v24,0(R1)         use v24 to test decoder
000012A4  E766 7200 8FBC                    627+         VGFMA V22,V22,V23,V24,2    test instruction (dest is a source)
000012AA  E760 5030 080E          00001268  628+         VST   V22,V1O3           save v1 output
000012B0  07FB                              629+         BR    R11               return
000012B4                                    630+RE3      DC    0F                xl16 expected result
000012B4                                    631+         DROP  R5
000012B4  00000001 00000000                632          DC    XL16'00000001000000000000000000000000'   expected result
000012BC  00000000 00000000
000012C4  80000000 00000000                633          DC    XL16'80000000000000000000000000000000'   v2
000012CC  00000000 00000000
000012D4  00000002 00000000                634          DC    XL16'00000002000000000000000000000000'   v3
000012DC  00000000 00000000
000012E4  00000000 00000000                635          DC    XL16'00000000000000000000000000000000'   v4
000012EC  00000000 00000000
                                            636
                                            637 * Doubleword
                                            638          VRR_D VGFMA,3
000012F8                                    639+         DS    0FD
000012F8                    000012F8        640+         USING *,R5              base for test data and test routine
000012F8  00001340                          641+T4       DC    A(X4)             address of test routine
000012FC  0004                              642+         DC    H'4'              test number
000012FE  00                                643+         DC    X'00'
000012FF  03                                644+         DC    HL1'3'            m5
00001300  E5C7C6D4 C1404040                 645+         DC    CL8'VGFMA'        instruction name
00001308  00001384                          646+         DC    A(RE4+16)         address of v2 source
0000130C  00001394                          647+         DC    A(RE4+32)         address of v3 source
00001310  000013A4                          648+         DC    A(RE4+48)         address of v4 source
00001314  00000010                          649+         DC    A(16)             result length
00001318  00001374                          650+REA4     DC    A(RE4)            result address
00001320  00000000 00000000                 651+         DS    FD                gap
00001328  00000000 00000000                 652+V1O4     DS    XL16              V1 output
00001330  00000000 00000000
00001338  00000000 00000000                 653+         DS    FD                gap
                                            654+*
00001340                                    655+X4       DS    0F
00001340  E310 5010 0014          00000010  656+         LGF   R1,V2ADDR         load v2 source
00001346  E761 0000 0806          00000000  657+         VL    v22,0(R1)         use v22 to test decoder
0000134C  E310 5014 0014          00000014  658+         LGF   R1,V3ADDR         load v3 source
00001352  E771 0000 0806          00000000  659+         VL    v23,0(R1)         use v23 to test decoder
00001358  E310 5018 0014          00000018  660+         LGF   R1,V4ADDR         load v4 source
0000135E  E781 0000 0806          00000000  661+         VL    v24,0(R1)         use v24 to test decoder
00001364  E766 7300 8FBC                    662+         VGFMA V22,V22,V23,V24,3    test instruction (dest is a source)
0000136A  E760 5030 080E          00001328  663+         VST   V22,V1O4           save v1 output
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001370  07FB                                      664+         BR    R11               return
00001374                                            665+RE4      DC    0F                xl16 expected result
00001374                                            666+         DROP  R5
00001374  00000000 00000001                         667          DC    XL16'00000000000000010000000000000000'   expected result
0000137C  00000000 00000000
00001384  80000000 00000000                         668          DC    XL16'80000000000000000000000000000000'   v2
0000138C  00000000 00000000
00001394  00000000 00000002                         669          DC    XL16'00000000000000020000000000000000'   v3
0000139C  00000000 00000000
000013A4  00000000 00000000                         670          DC    XL16'00000000000000000000000000000000'   v4
000013AC  00000000 00000000
                                                    671 *-------------------------------------------------------------------
                                                    672 * Byte
                                                    673          VRR_D VGFMA,0
000013B8                                            674+         DS    0FD
000013B8                          000013B8          675+         USING *,R5              base for test data and test routine
000013B8  00001400                                  676+T5       DC    A(X5)             address of test routine
000013BC  0005                                      677+         DC    H'5'              test number
000013BE  00                                        678+         DC    X'00'
000013BF  00                                        679+         DC    HL1'0'            m5
000013C0  E5C7C6D4 C1404040                         680+         DC    CL8'VGFMA'        instruction name
000013C8  00001444                                  681+         DC    A(RE5+16)         address of v2 source
000013CC  00001454                                  682+         DC    A(RE5+32)         address of v3 source
000013D0  00001464                                  683+         DC    A(RE5+48)         address of v4 source
000013D4  00000010                                  684+         DC    A(16)             result length
000013D8  00001434                                  685+REA5     DC    A(RE5)            result address
000013E0  00000000 00000000                         686+         DS    FD                gap
000013E8  00000000 00000000                         687+V1O5     DS    XL16              V1 output
000013F0  00000000 00000000
000013F8  00000000 00000000                         688+         DS    FD                gap
                                                    689+*
00001400                                            690+X5       DS    0F
00001400  E310 5010 0014                 00000010   691+         LGF   R1,V2ADDR         load v2 source
00001406  E761 0000 0806                 00000000   692+         VL    v22,0(R1)         use v22 to test decoder
0000140C  E310 5014 0014                 00000014   693+         LGF   R1,V3ADDR         load v3 source
00001412  E771 0000 0806                 00000000   694+         VL    v23,0(R1)         use v23 to test decoder
00001418  E310 5018 0014                 00000018   695+         LGF   R1,V4ADDR         load v4 source
0000141E  E781 0000 0806                 00000000   696+         VL    v24,0(R1)         use v24 to test decoder
00001424  E766 7000 8FBC                            697+         VGFMA V22,V22,V23,V24,0    test instruction (dest is a source)
0000142A  E760 5030 080E                 000013E8   698+         VST   V22,V1O5           save v1 output
00001430  07FB                                      699+         BR    R11               return
00001434                                            700+RE5      DC    0F                xl16 expected result
00001434                                            701+         DROP  R5
00001434  02000080 00000000                         702          DC    XL16'02000080000000000000000000000000'   expected result
0000143C  00000000 00000000
00001444  80008080 00000000                         703          DC    XL16'80008080000000000000000000000000'   v2
0000144C  00000000 00000000
00001454  02000203 00000000                         704          DC    XL16'02000203000000000000000000000000'   v3
0000145C  00000000 00000000
00001464  03000000 00000000                         705          DC    XL16'03000000000000000000000000000000'   v4
0000146C  00000000 00000000
                                                    706
                                                    707 * Halfword
                                                    708          VRR_D VGFMA,1
00001478                                            709+         DS    0FD
00001478                          00001478          710+         USING *,R5              base for test data and test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001478  000014C0                            711+T6       DC    A(X6)              address of test routine
0000147C  0006                                712+         DC    H'6'               test number
0000147E  00                                  713+         DC    X'00'
0000147F  01                                  714+         DC    HL1'1'             m5
00001480  E5C7C6D4 C1404040                   715+         DC    CL8'VGFMA'         instruction name
00001488  00001504                            716+         DC    A(RE6+16)          address of v2 source
0000148C  00001514                            717+         DC    A(RE6+32)          address of v3 source
00001490  00001524                            718+         DC    A(RE6+48)          address of v4 source
00001494  00000010                            719+         DC    A(16)              result length
00001498  000014F4                            720+REA6     DC    A(RE6)             result address
000014A0  00000000 00000000                   721+         DS    FD                 gap
000014A8  00000000 00000000                   722+V1O6     DS    XL16               V1 output
000014B0  00000000 00000000
000014B8  00000000 00000000                   723+         DS    FD                 gap
                                              724+*
000014C0                                      725+X6       DS    0F
000014C0  E310 5010 0014              00000010726+         LGF   R1,V2ADDR          load v2 source
000014C6  E761 0000 0806              00000000727+         VL    v22,0(R1)          use v22 to test decoder
000014CC  E310 5014 0014              00000014728+         LGF   R1,V3ADDR          load v3 source
000014D2  E771 0000 0806              00000000729+         VL    v23,0(R1)          use v23 to test decoder
000014D8  E310 5018 0014              00000018730+         LGF   R1,V4ADDR          load v4 source
000014DE  E781 0000 0806              00000000731+         VL    v24,0(R1)          use v24 to test decoder
000014E4  E766 7100 8FBC                      732+         VGFMA V22,V22,V23,V24,1    test instruction (dest is a source)
000014EA  E760 5030 080E              000014A8733+         VST   V22,V1O6            save v1 output
000014F0  07FB                                734+         BR    R11                return
000014F4                                      735+RE6      DC    0F                 xl16 expected result
000014F4                                      736+         DROP  R5
000014F4  00020000 00000000                   737          DC    XL16'00020000000000000000000000000000'   expected result
000014FC  00000000 00000000
00001504  80000000 00000000                   738          DC    XL16'80000000000000000000000000000000'   v2
0000150C  00000000 00000000
00001514  00020000 00000000                   739          DC    XL16'00020000000000000000000000000000'   v3
0000151C  00000000 00000000
00001524  00030000 00000000                   740          DC    XL16'00030000000000000000000000000000'   v4
0000152C  00000000 00000000
                                              741
                                              742 * Word
                                              743          VRR_D VGFMA,2
00001538                                      744+         DS    0FD
00001538                      00001538        745+         USING *,R5               base for test data and test routine
00001538  00001580                            746+T7       DC    A(X7)              address of test routine
0000153C  0007                                747+         DC    H'7'               test number
0000153E  00                                  748+         DC    X'00'
0000153F  02                                  749+         DC    HL1'2'             m5
00001540  E5C7C6D4 C1404040                   750+         DC    CL8'VGFMA'         instruction name
00001548  000015C4                            751+         DC    A(RE7+16)          address of v2 source
0000154C  000015D4                            752+         DC    A(RE7+32)          address of v3 source
00001550  000015E4                            753+         DC    A(RE7+48)          address of v4 source
00001554  00000010                            754+         DC    A(16)              result length
00001558  000015B4                            755+REA7     DC    A(RE7)             result address
00001560  00000000 00000000                   756+         DS    FD                 gap
00001568  00000000 00000000                   757+V1O7     DS    XL16               V1 output
00001570  00000000 00000000
00001578  00000000 00000000                   758+         DS    FD                 gap
                                              759+*
00001580                                      760+X7       DS    0F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001580  E310 5010 0014                 00000010   761+         LGF    R1,V2ADDR          load v2 source
00001586  E761 0000 0806                 00000000   762+         VL     v22,0(R1)          use v22 to test decoder
0000158C  E310 5014 0014                 00000014   763+         LGF    R1,V3ADDR          load v3 source
00001592  E771 0000 0806                 00000000   764+         VL     v23,0(R1)          use v23 to test decoder
00001598  E310 5018 0014                 00000018   765+         LGF    R1,V4ADDR          load v4 source
0000159E  E781 0000 0806                 00000000   766+         VL     v24,0(R1)          use v24 to test decoder
000015A4  E766 7200 8FBC                            767+         VGFMA  V22,V22,V23,V24,2    test instruction (dest is a source)
000015AA  E760 5030 080E                 00001568   768+         VST    V22,V1O7            save v1 output
000015B0  07FB                                      769+         BR     R11                return
000015B4                                            770+RE7      DC     0F                 xl16 expected result
000015B4                                            771+         DROP   R5
000015B4  00000002 00000000                         772          DC     XL16'00000002000000000000000000000000'   expected result
000015BC  00000000 00000000
000015C4  80000000 00000000                         773          DC     XL16'80000000000000000000000000000000'   v2
000015CC  00000000 00000000
000015D4  00000002 00000000                         774          DC     XL16'00000002000000000000000000000000'   v3
000015DC  00000000 00000000
000015E4  00000003 00000000                         775          DC     XL16'00000003000000000000000000000000'   v4
000015EC  00000000 00000000
                                                    776
                                                    777 * Doubleword
                                                    778          VRR_D  VGFMA,3
000015F8                                            779+         DS     0FD
000015F8                          000015F8          780+         USING  *,R5               base for test data and test routine
000015F8  00001640                                  781+T8       DC     A(X8)              address of test routine
000015FC  0008                                      782+         DC     H'8'               test number
000015FE  00                                        783+         DC     X'00'
000015FF  03                                        784+         DC     HL1'3'             m5
00001600  E5C7C6D4 C1404040                         785+         DC     CL8'VGFMA'         instruction name
00001608  00001684                                  786+         DC     A(RE8+16)          address of v2 source
0000160C  00001694                                  787+         DC     A(RE8+32)          address of v3 source
00001610  000016A4                                  788+         DC     A(RE8+48)          address of v4 source
00001614  00000010                                  789+         DC     A(16)              result length
00001618  00001674                                  790+REA8     DC     A(RE8)             result address
00001620  00000000 00000000                         791+         DS     FD                 gap
00001628  00000000 00000000                         792+V1O8     DS     XL16               V1 output
00001630  00000000 00000000
00001638  00000000 00000000                         793+         DS     FD                 gap
                                                    794+*
00001640                                            795+X8       DS     0F
00001640  E310 5010 0014                 00000010   796+         LGF    R1,V2ADDR          load v2 source
00001646  E761 0000 0806                 00000000   797+         VL     v22,0(R1)          use v22 to test decoder
0000164C  E310 5014 0014                 00000014   798+         LGF    R1,V3ADDR          load v3 source
00001652  E771 0000 0806                 00000000   799+         VL     v23,0(R1)          use v23 to test decoder
00001658  E310 5018 0014                 00000018   800+         LGF    R1,V4ADDR          load v4 source
0000165E  E781 0000 0806                 00000000   801+         VL     v24,0(R1)          use v24 to test decoder
00001664  E766 7300 8FBC                            802+         VGFMA  V22,V22,V23,V24,3    test instruction (dest is a source)
0000166A  E760 5030 080E                 00001628   803+         VST    V22,V1O8            save v1 output
00001670  07FB                                      804+         BR     R11                return
00001674                                            805+RE8      DC     0F                 xl16 expected result
00001674                                            806+         DROP   R5
00001674  00000000 00000002                         807          DC     XL16'00000000000000020000000000000000'   expected result
0000167C  00000000 00000000
00001684  80000000 00000000                         808          DC     XL16'80000000000000000000000000000000'   v2
0000168C  00000000 00000000
00001694  00000000 00000002                         809          DC     XL16'00000000000000020000000000000000'   v3
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000169C  00000000 00000000
000016A4  00000000 00000003                          810          DC    XL16'00000000000000030000000000000000'   v4
000016AC  00000000 00000000
                                                     811 *-------------------------------------------------------------------
                                                     812 * case 1
                                                     813 *-------------------------------------------------------------------
                                                     814 * Byte
                                                     815          VRR_D VGFMA,0
000016B8                                             816+         DS    0FD
000016B8                       000016B8              817+         USING *,R5              base for test data and test routine
000016B8  00001700                                   818+T9       DC    A(X9)             address of test routine
000016BC  0009                                       819+         DC    H'9'              test number
000016BE  00                                         820+         DC    X'00'
000016BF  00                                         821+         DC    HL1'0'            m5
000016C0  E5C7C6D4 C1404040                          822+         DC    CL8'VGFMA'        instruction name
000016C8  00001744                                   823+         DC    A(RE9+16)         address of v2 source
000016CC  00001754                                   824+         DC    A(RE9+32)         address of v3 source
000016D0  00001764                                   825+         DC    A(RE9+48)         address of v4 source
000016D4  00000010                                   826+         DC    A(16)             result length
000016D8  00001734                                   827+REA9     DC    A(RE9)            result address
000016E0  00000000 00000000                          828+         DS    FD                gap
000016E8  00000000 00000000                          829+V1O9     DS    XL16              V1 output
000016F0  00000000 00000000
000016F8  00000000 00000000                          830+         DS    FD                gap
                                                     831+*
00001700                                             832+X9       DS    0F
00001700  E310 5010 0014                 00000010    833+         LGF   R1,V2ADDR         load v2 source
00001706  E761 0000 0806                 00000000    834+         VL    v22,0(R1)         use v22 to test decoder
0000170C  E310 5014 0014                 00000014    835+         LGF   R1,V3ADDR         load v3 source
00001712  E771 0000 0806                 00000000    836+         VL    v23,0(R1)         use v23 to test decoder
00001718  E310 5018 0014                 00000018    837+         LGF   R1,V4ADDR         load v4 source
0000171E  E781 0000 0806                 00000000    838+         VL    v24,0(R1)         use v24 to test decoder
00001724  E766 7000 8FBC                             839+         VGFMA V22,V22,V23,V24,0    test instruction (dest is a source)
0000172A  E760 5030 080E                 000016E8    840+         VST   V22,V1O9           save v1 output
00001730  07FB                                       841+         BR    R11               return
00001734                                             842+RE9      DC    0F                xl16 expected result
00001734                                             843+         DROP  R5
00001734  58407242 74447646                          844          DC    XL16'584072427444764678487A4A7C4C7E4E'   expected result
0000173C  78487A4A 7C4C7E4E
00001744  50515253 54555657                          845          DC    XL16'505152535455565758595A5B5C5D5E5F'   v2
0000174C  58595A5B 5C5D5E5F
00001754  E0616263 64656667                          846          DC    XL16'E061626364656667686 96A6B6C6D6E6F'   v3
0000175C  68696A6B 6C6D6E6F
00001764  70717273 74757677                          847          DC    XL16'707172737475767778797A7B7C7D7E7F'   v4
0000176C  78797A7B 7C7D7E7F
                                                     848
                                                     849 * Halfword
                                                     850          VRR_D VGFMA,1
00001778                                             851+         DS    0FD
00001778                       00001778              852+         USING *,R5              base for test data and test routine
00001778  000017C0                                   853+T10      DC    A(X10)            address of test routine
0000177C  000A                                       854+         DC    H'10'             test number
0000177E  00                                         855+         DC    X'00'
0000177F  01                                         856+         DC    HL1'1'            m5
00001780  E5C7C6D4 C1404040                          857+         DC    CL8'VGFMA'        instruction name
00001788  00001804                                   858+         DC    A(RE10+16)        address of v2 source
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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

0000178C  00001814                              859+         DC    A(RE10+32)        address of v3 source
00001790  00001824                              860+         DC    A(RE10+48)        address of v4 source
00001794  00000010                              861+         DC    A(16)             result length
00001798  000017F4                              862+REA10    DC    A(RE10)           result address
000017A0  00000000 00000000                     863+         DS    FD                gap
000017A8  00000000 00000000                     864+V1O10    DS    XL16              V1 output
000017B0  00000000 00000000
000017B8  00000000 00000000                     865+         DS    FD                gap
                                                866+*
000017C0                                        867+X10      DS    0F
000017C0  E310 5010 0014              00000010  868+         LGF   R1,V2ADDR         load v2 source
000017C6  E761 0000 0806              00000000  869+         VL    v22,0(R1)         use v22 to test decoder
000017CC  E310 5014 0014              00000014  870+         LGF   R1,V3ADDR         load v3 source
000017D2  E771 0000 0806              00000000  871+         VL    v23,0(R1)         use v23 to test decoder
000017D8  E310 5018 0014              00000018  872+         LGF   R1,V4ADDR         load v4 source
000017DE  E781 0000 0806              00000000  873+         VL    v24,0(R1)         use v24 to test decoder
000017E4  E766 7100 8FBC                        874+         VGFMA V22,V22,V23,V24,1    test instruction (dest is a source)
000017EA  E760 5030 080E              000017A8  875+         VST   V22,V1O10          save v1 output
000017F0  07FB                                  876+         BR    R11               return
000017F4                                        877+RE10     DC    0F                xl16 expected result
000017F4                                        878+         DROP  R5
000017F4  583DF217 74117613                     879          DC    XL16'583DF21774117613781D7A1F7C197E1B'   expected result
000017FC  781D7A1F 7C197E1B
00001804  50515253 54555657                     880          DC    XL16'505152535455565758595A5B5C5D5E5F'   v2
0000180C  58595A5B 5C5D5E5F
00001814  E0616263 64656667                     881          DC    XL16'E061626364656667686969A6B6C6D6E6F'   v3
0000181C  68696A6B 6C6D6E6F
00001824  70717273 74757677                     882          DC    XL16'707172737475767778797A7B7C7D7E7F'   v4
0000182C  78797A7B 7C7D7E7F
                                                883
                                                884 * Word
                                                885          VRR_D VGFMA,2
00001838                                        886+         DS    0FD
00001838                      00001838          887+         USING *,R5              base for test data and test routine
00001838  00001880                              888+T11      DC    A(X11)            address of test routine
0000183C  000B                                  889+         DC    H'11'             test number
0000183E  00                                    890+         DC    X'00'
0000183F  02                                    891+         DC    HL1'2'            m5
00001840  E5C7C6D4 C1404040                     892+         DC    CL8'VGFMA'        instruction name
00001848  000018C4                              893+         DC    A(RE11+16)        address of v2 source
0000184C  000018D4                              894+         DC    A(RE11+32)        address of v3 source
00001850  000018E4                              895+         DC    A(RE11+48)        address of v4 source
00001854  00000010                              896+         DC    A(16)             result length
00001858  000018B4                              897+REA11    DC    A(RE11)           result address
00001860  00000000 00000000                     898+         DS    FD                gap
00001868  00000000 00000000                     899+V1O11    DS    XL16              V1 output
00001870  00000000 00000000
00001878  00000000 00000000                     900+         DS    FD                gap
                                                901+*
00001880                                        902+X11      DS    0F
00001880  E310 5010 0014              00000010  903+         LGF   R1,V2ADDR         load v2 source
00001886  E761 0000 0806              00000000  904+         VL    v22,0(R1)         use v22 to test decoder
0000188C  E310 5014 0014              00000014  905+         LGF   R1,V3ADDR         load v3 source
00001892  E771 0000 0806              00000000  906+         VL    v23,0(R1)         use v23 to test decoder
00001898  E310 5018 0014              00000018  907+         LGF   R1,V4ADDR         load v4 source
0000189E  E781 0000 0806              00000000  908+         VL    v24,0(R1)         use v24 to test decoder
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000018A4  E766 7200 8FBC                           909+         VGFMA V22,V22,V23,V24,2    test instruction (dest is a source)
000018AA  E760 5030 080E                 00001868  910+         VST   V22,V1O11           save v1 output
000018B0  07FB                                     911+         BR    R11                 return
000018B4                                           912+RE11     DC    0F                  xl16 expected result
000018B4                                           913+         DROP  R5
000018B4  5889DB8A F4A576A7                        914          DC    XL16'5889DB8AF4A576A778A97AAB7CAD7EAF'   expected result
000018BC  78A97AAB 7CAD7EAF
000018C4  50515253 54555657                        915          DC    XL16'505152535455565758595A5B5C5D5E5F'   v2
000018CC  58595A5B 5C5D5E5F
000018D4  E0616263 64656667                        916          DC    XL16'E06162636465666768696A6B6C6D6E6F'   v3
000018DC  68696A6B 6C6D6E6F
000018E4  70717273 74757677                        917          DC    XL16'70717273747576777879 7A7B7C7D7E7F'  v4
000018EC  78797A7B 7C7D7E7F
                                                   918
                                                   919 * Doubleword
                                                   920          VRR_D VGFMA,3
000018F8                                           921+         DS    0FD
000018F8                           000018F8        922+         USING *,R5                base for test data and test routine
000018F8  00001940                                 923+T12      DC    A(X12)              address of test routine
000018FC  000C                                     924+         DC    H'12'               test number
000018FE  00                                       925+         DC    X'00'
000018FF  03                                       926+         DC    HL1'3'              m5
00001900  E5C7C6D4 C1404040                        927+         DC    CL8'VGFMA'          instruction name
00001908  00001984                                 928+         DC    A(RE12+16)          address of v2 source
0000190C  00001994                                 929+         DC    A(RE12+32)          address of v3 source
00001910  000019A4                                 930+         DC    A(RE12+48)          address of v4 source
00001914  00000010                                 931+         DC    A(16)               result length
00001918  00001974                                 932+REA12    DC    A(RE12)             result address
00001920  00000000 00000000                        933+         DS    FD                  gap
00001928  00000000 00000000                        934+V1O12    DS    XL16                V1 output
00001930  00000000 00000000
00001938  00000000 00000000                        935+         DS    FD                  gap
                                                   936+*
00001940                                           937+X12      DS    0F
00001940  E310 5010 0014                 00000010  938+         LGF   R1,V2ADDR           load v2 source
00001946  E761 0000 0806                 00000000  939+         VL    v22,0(R1)           use v22 to test decoder
0000194C  E310 5014 0014                 00000014  940+         LGF   R1,V3ADDR           load v3 source
00001952  E771 0000 0806                 00000000  941+         VL    v23,0(R1)           use v23 to test decoder
00001958  E310 5018 0014                 00000018  942+         LGF   R1,V4ADDR           load v4 source
0000195E  E781 0000 0806                 00000000  943+         VL    v24,0(R1)           use v24 to test decoder
00001964  E766 7300 8FBC                           944+         VGFMA V22,V22,V23,V24,3    test instruction (dest is a source)
0000196A  E760 5030 080E                 00001928  945+         VST   V22,V1O12           save v1 output
00001970  07FB                                     946+         BR    R11                 return
00001974                                           947+RE12     DC    0F                  xl16 expected result
00001974                                           948+         DROP  R5
00001974  5999DA9A DF9FDC9C                        949          DC    XL16'5999DA9ADF9FDC9CF9B97BBB7DBD7FBF'   expected result
0000197C  F9B97BBB 7DBD7FBF
00001984  50515253 54555657                        950          DC    XL16'505152535455565758595A5B5C5D5E5F'   v2
0000198C  58595A5B 5C5D5E5F
00001994  E0616263 64656667                        951          DC    XL16'E06162636465666768696A6B6C6D6E6F'   v3
0000199C  68696A6B 6C6D6E6F
000019A4  70717273 74757677                        952          DC    XL16'70717273747576777879 7A7B7C7D7E7F'  v4
000019AC  78797A7B 7C7D7E7F
                                                   953
                                                   954 *-------------------------------------------------------------------
                                                   955 * case 2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    956 *-------------------------------------------------------------------
                                                    957 * Byte
                                                    958          VRR_D VGFMA,0
000019B8                                            959+         DS    0FD
000019B8                      000019B8              960+         USING *,R5              base for test data and test routine
000019B8  00001A00                                  961+T13      DC    A(X13)            address of test routine
000019BC  000D                                      962+         DC    H'13'             test number
000019BE  00                                        963+         DC    X'00'
000019BF  00                                        964+         DC    HL1'0'            m5
000019C0  E5C7C6D4 C1404040                         965+         DC    CL8'VGFMA'        instruction name
000019C8  00001A44                                  966+         DC    A(RE13+16)        address of v2 source
000019CC  00001A54                                  967+         DC    A(RE13+32)        address of v3 source
000019D0  00001A64                                  968+         DC    A(RE13+48)        address of v4 source
000019D4  00000010                                  969+         DC    A(16)             result length
000019D8  00001A34                                  970+REA13    DC    A(RE13)           result address
000019E0  00000000 00000000                         971+         DS    FD                gap
000019E8  00000000 00000000                         972+V1O13    DS    XL16              V1 output
000019F0  00000000 00000000
000019F8  00000000 00000000                         973+         DS    FD                gap
                                                    974+*
00001A00                                            975+X13      DS    0F
00001A00  E310 5010 0014              00000010      976+         LGF   R1,V2ADDR         load v2 source
00001A06  E761 0000 0806              00000000      977+         VL    v22,0(R1)         use v22 to test decoder
00001A0C  E310 5014 0014              00000014      978+         LGF   R1,V3ADDR         load v3 source
00001A12  E771 0000 0806              00000000      979+         VL    v23,0(R1)         use v23 to test decoder
00001A18  E310 5018 0014              00000018      980+         LGF   R1,V4ADDR         load v4 source
00001A1E  E781 0000 0806              00000000      981+         VL    v24,0(R1)         use v24 to test decoder
00001A24  E766 7000 8FBC                            982+         VGFMA V22,V22,V23,V24,0    test instruction (dest is a source)
00001A2A  E760 5030 080E              000019E8      983+         VST   V22,V1O13          save v1 output
00001A30  07FB                                      984+         BR    R11               return
00001A34                                            985+RE13     DC    0F                xl16 expected result
00001A34                                            986+         DROP  R5
00001A34  75977795 71937391                         987          DC    XL16'7597779571937391D9F7F9D799B7961'   expected result
00001A3C  7D9F7F9D 799B7961
00001A44  50515253 54555657                         988          DC    XL16'505152535455565758595A5B5C5D5E5F'   v2
00001A4C  58595A5B 5C5D5E5F
00001A54  F6E6D6C6 B6A69686                         989          DC    XL16'F6E6D6C6B6A6968676656463626160E'   v3
00001A5C  76665646 3626160E
00001A64  70717273 74757677                         990          DC    XL16'70717273747576778797A7B7C7D7E7F'   v4
00001A6C  78797A7B 7C7D7E7F
                                                    991
                                                    992 * Halfword
                                                    993          VRR_D VGFMA,1
00001A78                                            994+         DS    0FD
00001A78                      00001A78              995+         USING *,R5              base for test data and test routine
00001A78  00001AC0                                  996+T14      DC    A(X14)            address of test routine
00001A7C  000E                                      997+         DC    H'14'             test number
00001A7E  00                                        998+         DC    X'00'
00001A7F  01                                        999+         DC    HL1'1'            m5
00001A80  E5C7C6D4 C1404040                        1000+         DC    CL8'VGFMA'        instruction name
00001A88  00001B04                                 1001+         DC    A(RE14+16)        address of v2 source
00001A8C  00001B14                                 1002+         DC    A(RE14+32)        address of v3 source
00001A90  00001B24                                 1003+         DC    A(RE14+48)        address of v4 source
00001A94  00000010                                 1004+         DC    A(16)             result length
00001A98  00001AF4                                 1005+REA14    DC    A(RE14)           result address
00001AA0  00000000 00000000                        1006+         DS    FD                gap
```

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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00001AA8  00000000 00000000                       1007+V1O14    DS    XL16              V1 output
00001AB0  00000000 00000000
00001AB8  00000000 00000000                       1008+         DS    FD                gap
                                                  1009+*
00001AC0                                          1010+X14      DS    0F
00001AC0  E310 5010 0014                 00000010 1011+         LGF   R1,V2ADDR         load v2 source
00001AC6  E761 0000 0806                 00000000 1012+         VL    v22,0(R1)         use v22 to test decoder
00001ACC  E310 5014 0014                 00000014 1013+         LGF   R1,V3ADDR         load v3 source
00001AD2  E771 0000 0806                 00000000 1014+         VL    v23,0(R1)         use v23 to test decoder
00001AD8  E310 5018 0014                 00000018 1015+         LGF   R1,V4ADDR         load v4 source
00001ADE  E781 0000 0806                 00000000 1016+         VL    v24,0(R1)         use v24 to test decoder
00001AE4  E766 7100 8FBC                          1017+         VGFMA V22,V22,V23,V24,1    test instruction (dest is a source)
00001AEA  E760 5030 080E                 00001AA8 1018+         VST   V22,V1O14          save v1 output
00001AF0  07FB                                    1019+         BR    R11               return
00001AF4                                          1020+RE14     DC    0F                xl16 expected result
00001AF4                                          1021+         DROP  R5
00001AF4  7BDD79DF 7FD97DDB                       1022          DC    XL16'7BDD79DF7FD97DDB73D571D777D3872B'   expected result
00001AFC  73D571D7 77D3872B
00001B04  50515253 54555657                       1023          DC    XL16'505152535455565758595A5B5C5D5E5F'   v2
00001B0C  58595A5B 5C5D5E5F
00001B14  F6E6D6C6 B6A69686                       1024          DC    XL16'F6E6D6C6B6A6968676665646362616 0E'   v3
00001B1C  76665646 3626160E
00001B24  70717273 74757677                       1025          DC    XL16'707172737475767778797A7B7C7D7E7F'   v4
00001B2C  78797A7B 7C7D7E7F
                                                  1026
                                                  1027 * Word
                                                  1028          VRR_D VGFMA,2
00001B38                                          1029+         DS    0FD
00001B38                          00001B38        1030+         USING *,R5              base for test data and test routine
00001B38  00001B80                                1031+T15      DC    A(X15)            address of test routine
00001B3C  000F                                    1032+         DC    H'15'             test number
00001B3E  00                                      1033+         DC    X'00'
00001B3F  02                                      1034+         DC    HL1'2'            m5
00001B40  E5C7C6D4 C1404040                       1035+         DC    CL8'VGFMA'        instruction name
00001B48  00001BC4                                1036+         DC    A(RE15+16)        address of v2 source
00001B4C  00001BD4                                1037+         DC    A(RE15+32)        address of v3 source
00001B50  00001BE4                                1038+         DC    A(RE15+48)        address of v4 source
00001B54  00000010                                1039+         DC    A(16)             result length
00001B58  00001BB4                                1040+REA15    DC    A(RE15)           result address
00001B60  00000000 00000000                       1041+         DS    FD                gap
00001B68  00000000 00000000                       1042+V1O15    DS    XL16              V1 output
00001B70  00000000 00000000
00001B78  00000000 00000000                       1043+         DS    FD                gap
                                                  1044+*
00001B80                                          1045+X15      DS    0F
00001B80  E310 5010 0014                 00000010 1046+         LGF   R1,V2ADDR         load v2 source
00001B86  E761 0000 0806                 00000000 1047+         VL    v22,0(R1)         use v22 to test decoder
00001B8C  E310 5014 0014                 00000014 1048+         LGF   R1,V3ADDR         load v3 source
00001B92  E771 0000 0806                 00000000 1049+         VL    v23,0(R1)         use v23 to test decoder
00001B98  E310 5018 0014                 00000018 1050+         LGF   R1,V4ADDR         load v4 source
00001B9E  E781 0000 0806                 00000000 1051+         VL    v24,0(R1)         use v24 to test decoder
00001BA4  E766 7200 8FBC                          1052+         VGFMA V22,V22,V23,V24,2    test instruction (dest is a source)
00001BAA  E760 5030 080E                 00001B68 1053+         VST   V22,V1O15          save v1 output
00001BB0  07FB                                    1054+         BR    R11               return
00001BB4                                          1055+RE15     DC    0F                xl16 expected result
00001BB4                                          1056+         DROP  R5
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001BB4  66A964AB 62AD60AF                        1057          DC    XL16'66A964AB62AD60AF6EA16CA1884F9A5F'   expected result
00001BBC  6EA16CA1 884F9A5F
00001BC4  50515253 54555657                        1058          DC    XL16'505152535455565758595A5B5C5D5E5F'   v2
00001BCC  58595A5B 5C5D5E5F
00001BD4  F6E6D6C6 B6A69686                        1059          DC    XL16'F6E6D6C6B6A6968676665646362616 0E'   v3
00001BDC  76665646 3626160E
00001BE4  70717273 74757677                        1060          DC    XL16'707172737475767778797A7B7C7D7E7F'   v4
00001BEC  78797A7B 7C7D7E7F
                                                   1061
                                                   1062 * Doubleword
                                                   1063          VRR_D VGFMA,3
00001BF8                                           1064+         DS    0FD
00001BF8                     00001BF8              1065+         USING *,R5              base for test data and test routine
00001BF8  00001C40                                 1066+T16      DC    A(X16)            address of test routine
00001BFC  0010                                     1067+         DC    H'16'             test number
00001BFE  00                                       1068+         DC    X'00'
00001BFF  03                                       1069+         DC    HL1'3'            m5
00001C00  E5C7C6D4 C1404040                        1070+         DC    CL8'VGFMA'        instruction name
00001C08  00001C84                                 1071+         DC    A(RE16+16)        address of v2 source
00001C0C  00001C94                                 1072+         DC    A(RE16+32)        address of v3 source
00001C10  00001CA4                                 1073+         DC    A(RE16+48)        address of v4 source
00001C14  00000010                                 1074+         DC    A(16)             result length
00001C18  00001C74                                 1075+REA16    DC    A(RE16)           result address
00001C20  00000000 00000000                        1076+         DS    FD                gap
00001C28  00000000 00000000                        1077+V1O16    DS    XL16              V1 output
00001C30  00000000 00000000
00001C38  00000000 00000000                        1078+         DS    FD                gap
                                                   1079+*
00001C40                                           1080+X16      DS    0F
00001C40  E310 5010 0014              00000010     1081+         LGF   R1,V2ADDR         load v2 source
00001C46  E761 0000 0806              00000000     1082+         VL    v22,0(R1)         use v22 to test decoder
00001C4C  E310 5014 0014              00000014     1083+         LGF   R1,V3ADDR         load v3 source
00001C52  E771 0000 0806              00000000     1084+         VL    v23,0(R1)         use v23 to test decoder
00001C58  E310 5018 0014              00000018     1085+         LGF   R1,V4ADDR         load v4 source
00001C5E  E781 0000 0806              00000000     1086+         VL    v24,0(R1)         use v24 to test decoder
00001C64  E766 7300 8FBC                           1087+         VGFMA V22,V22,V23,V24,3    test instruction (dest is a source)
00001C6A  E760 5030 080E              00001C28     1088+         VST   V22,V1O16          save v1 output
00001C70  07FB                                     1089+         BR    R11               return
00001C74                                           1090+RE16     DC    0F                xl16 expected result
00001C74                                           1091+         DROP  R5
00001C74  5BC159C3 5FC55DC5                        1092          DC    XL16'5BC159C35FC55DC591038311B527A737'   expected result
00001C7C  91038311 B527A737
00001C84  50515253 54555657                        1093          DC    XL16'505152535455565758595A5B5C5D5E5F'   v2
00001C8C  58595A5B 5C5D5E5F
00001C94  F6E6D6C6 B6A69686                        1094          DC    XL16'F6E6D6C6B6A6968676665646362616 0E'   v3
00001C9C  76665646 3626160E
00001CA4  70717273 74757677                        1095          DC    XL16'707172737475767778797A7B7C7D7E7F'   v4
00001CAC  78797A7B 7C7D7E7F
                                                   1096
                                                   1097
                                                   1098
00001CB4  00000000                                 1099          DC    F'0'     END OF TABLE
00001CB8  00000000                                 1100          DC    F'0'
                                                   1101 *
                                                   1102 * table of pointers to individual load test
                                                   1103 *
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00001CBC                                          1104 E7TESTS  DS    0F
                                                  1105          PTTABLE
00001CBC                                          1106+TTABLE   DS    0F
00001CBC  000010B8                                1107+         DC    A(T1)              TEST &CUR
00001CC0  00001178                                1108+         DC    A(T2)              TEST &CUR
00001CC4  00001238                                1109+         DC    A(T3)              TEST &CUR
00001CC8  000012F8                                1110+         DC    A(T4)              TEST &CUR
00001CCC  000013B8                                1111+         DC    A(T5)              TEST &CUR
00001CD0  00001478                                1112+         DC    A(T6)              TEST &CUR
00001CD4  00001538                                1113+         DC    A(T7)              TEST &CUR
00001CD8  000015F8                                1114+         DC    A(T8)              TEST &CUR
00001CDC  000016B8                                1115+         DC    A(T9)              TEST &CUR
00001CE0  00001778                                1116+         DC    A(T10)             TEST &CUR
00001CE4  00001838                                1117+         DC    A(T11)             TEST &CUR
00001CE8  000018F8                                1118+         DC    A(T12)             TEST &CUR
00001CEC  000019B8                                1119+         DC    A(T13)             TEST &CUR
00001CF0  00001A78                                1120+         DC    A(T14)             TEST &CUR
00001CF4  00001B38                                1121+         DC    A(T15)             TEST &CUR
00001CF8  00001BF8                                1122+         DC    A(T16)             TEST &CUR
                                                  1123+*
00001CFC  00000000                                1124+         DC    A(0)               END OF TABLE
00001D00  00000000                                1125+         DC    A(0)
                                                  1126
00001D04  00000000                                1127          DC    F'0'     END OF TABLE
00001D08  00000000                                1128          DC    F'0'
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                 1130 ********************************************************************************
                                                 1131 *        Register equates
                                                 1132 ********************************************************************************


                             00000000  00000001  1134 R0       EQU   0
                             00000001  00000001  1135 R1       EQU   1
                             00000002  00000001  1136 R2       EQU   2
                             00000003  00000001  1137 R3       EQU   3
                             00000004  00000001  1138 R4       EQU   4
                             00000005  00000001  1139 R5       EQU   5
                             00000006  00000001  1140 R6       EQU   6
                             00000007  00000001  1141 R7       EQU   7
                             00000008  00000001  1142 R8       EQU   8
                             00000009  00000001  1143 R9       EQU   9
                             0000000A  00000001  1144 R10      EQU   10
                             0000000B  00000001  1145 R11      EQU   11
                             0000000C  00000001  1146 R12      EQU   12
                             0000000D  00000001  1147 R13      EQU   13
                             0000000E  00000001  1148 R14      EQU   14
                             0000000F  00000001  1149 R15      EQU   15


                                                 1151 ********************************************************************************
                                                 1152 *        Register equates
                                                 1153 ********************************************************************************


                          00000000  00000001  1155 V0       EQU   0
                          00000001  00000001  1156 V1       EQU   1
                          00000002  00000001  1157 V2       EQU   2
                          00000003  00000001  1158 V3       EQU   3
                          00000004  00000001  1159 V4       EQU   4
                          00000005  00000001  1160 V5       EQU   5
                          00000006  00000001  1161 V6       EQU   6
                          00000007  00000001  1162 V7       EQU   7
                          00000008  00000001  1163 V8       EQU   8
                          00000009  00000001  1164 V9       EQU   9
                          0000000A  00000001  1165 V10      EQU   10
                          0000000B  00000001  1166 V11      EQU   11
                          0000000C  00000001  1167 V12      EQU   12
                          0000000D  00000001  1168 V13      EQU   13
                          0000000E  00000001  1169 V14      EQU   14
                          0000000F  00000001  1170 V15      EQU   15
                          00000010  00000001  1171 V16      EQU   16
                          00000011  00000001  1172 V17      EQU   17
                          00000012  00000001  1173 V18      EQU   18
                          00000013  00000001  1174 V19      EQU   19
                          00000014  00000001  1175 V20      EQU   20
                          00000015  00000001  1176 V21      EQU   21
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                00000016  00000001  1177 V22       EQU   22
                                00000017  00000001  1178 V23       EQU   23
                                00000018  00000001  1179 V24       EQU   24
                                00000019  00000001  1180 V25       EQU   25
                                0000001A  00000001  1181 V26       EQU   26
                                0000001B  00000001  1182 V27       EQU   27
                                0000001C  00000001  1183 V28       EQU   28
                                0000001D  00000001  1184 V29       EQU   29
                                0000001E  00000001  1185 V30       EQU   30
                                0000001F  00000001  1186 V31       EQU   31
                                                    1187
                                                    1188           END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
BEGIN	I	00000200	2	151	117 147 148 149
CTLR0	F	0000048C	4	347	161 162 163 164
DECNUM	C	00001073	16	398	261 263 269 271
E7TEST	4	00000000	72	412	210
E7TESTS	F	00001CBC	4	1104	203
EDIT	X	00001047	18	393	262 270
ENDTEST	U	0000031E	1	247	208
EOJ	I	00000470	4	337	196 250
EOJPSW	D	00000460	8	335	337
FAILCONT	U	0000030E	1	237	
FAILED	F	00001000	4	375	239 248
FAILMSG	U	0000030A	1	231	221
FAILPSW	D	00000478	8	339	341
FAILTEST	I	00000488	4	341	251
FB0001	F	00000280	8	180	184 185 187
IMAGE	1	00000000	7436	0	
K	U	00000400	1	359	360 361 362
K64	U	00010000	1	361	
M5	U	00000007	1	416	268
MB	U	00100000	1	362	
MSG	I	000003A8	4	297	195 280
MSGCMD	C	000003F6	9	327	310 311
MSGMSG	C	000003FF	95	328	304 325 302
MSGMVC	I	000003F0	6	325	308
MSGOK	I	000003BE	2	306	303
MSGRET	I	000003DE	4	321	314 317
MSGSAVE	F	000003E4	4	324	300 321
NEXTE6	U	000002D4	1	205	224 242
OPNAME	C	00000008	8	418	266
PAGE	U	00001000	1	360	
PRT3	C	0000105D	18	396	262 263 264 270 271 272
PRTLINE	C	00001008	16	381	388 279
PRTLNG	U	0000003F	1	388	278
PRTM5	C	00001044	2	386	272
PRTNAME	C	00001033	8	384	266
PRTNUM	C	00001018	3	382	264
R0	U	00000000	1	1134	111 161 164 184 186 187 188 193 212 213 238 239 277
					278 281 297 300 302 304 306 321
R1	U	00000001	1	1135	194 219 220 248 249 279 311 325 551 552 553 554 555
					556 586 587 588 589 590 591 621 622 623 624 625 626
					656 657 658 659 660 661 691 692 693 694 695 696 726
					727 728 729 730 731 761 762 763 764 765 766 796 797
					798 799 800 801 833 834 835 836 837 838 868 869 870
					871 872 873 903 904 905 906 907 908 938 939 940 941
					942 943 976 977 978 979 980 981 1011 1012 1013 1014 1015
					1016 1046 1047 1048 1049 1050 1051 1081 1082 1083 1084 1085 1086
R10	U	0000000A	1	1144	149 158 159
R11	U	0000000B	1	1145	216 217 559 594 629 664 699 734 769 804 841 876 911
					946 984 1019 1054 1089
R12	U	0000000C	1	1146	203 206 223 241
R13	U	0000000D	1	1147	
R14	U	0000000E	1	1148	
R15	U	0000000F	1	1149	232 257 284 285
R2	U	00000002	1	1136	195 260 261 268 269 277 280 281 298 300 306 307 308
					310 316 321 322
R3	U	00000003	1	1137	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
R4	U	00000004	1	1138	
R5	U	00000005	1	1139	206 207 210 258 283 535 561 570 596 605 631 640 666 675 701 710 736 745 771 780 806 817 843 852 878 887 913 922 948 960 986 995 1021 1030 1056 1065 1091
R6	U	00000006	1	1140	
R7	U	00000007	1	1141	
R8	U	00000008	1	1142	147 151 152 153 155
R9	U	00000009	1	1143	148 155 156 158
RE1	F	00001134	4	560	541 542 543 545
RE10	F	000017F4	4	877	858 859 860 862
RE11	F	000018B4	4	912	893 894 895 897
RE12	F	00001974	4	947	928 929 930 932
RE13	F	00001A34	4	985	966 967 968 970
RE14	F	00001AF4	4	1020	1001 1002 1003 1005
RE15	F	00001BB4	4	1055	1036 1037 1038 1040
RE16	F	00001C74	4	1090	1071 1072 1073 1075
RE2	F	000011F4	4	595	576 577 578 580
RE3	F	000012B4	4	630	611 612 613 615
RE4	F	00001374	4	665	646 647 648 650
RE5	F	00001434	4	700	681 682 683 685
RE6	F	000014F4	4	735	716 717 718 720
RE7	F	000015B4	4	770	751 752 753 755
RE8	F	00001674	4	805	786 787 788 790
RE9	F	00001734	4	842	823 824 825 827
REA1	A	000010D8	4	545	
REA10	A	00001798	4	862	
REA11	A	00001858	4	897	
REA12	A	00001918	4	932	
REA13	A	000019D8	4	970	
REA14	A	00001A98	4	1005	
REA15	A	00001B58	4	1040	
REA16	A	00001C18	4	1075	
REA2	A	00001198	4	580	
REA3	A	00001258	4	615	
REA4	A	00001318	4	650	
REA5	A	000013D8	4	685	
REA6	A	00001498	4	720	
REA7	A	00001558	4	755	
REA8	A	00001618	4	790	
REA9	A	000016D8	4	827	
READDR	A	00000020	4	423	219
REG2LOW	U	000000DD	1	365	
REG2PATT	U	AABBCCDD	1	364	
RELEN	A	0000001C	4	422	
RPTDWSAV	D	00000398	8	290	277 281
RPTERROR	I	0000032C	4	257	232
RPTSAVE	F	00000390	4	287	257 284
RPTSVR5	F	00000394	4	288	258 283
SKL0001	U	0000004E	1	177	193
SKT0001	C	0000022A	20	174	177 194
SVOLDPSW	U	00000140	0	113	
T1	A	000010B8	4	536	1107
T10	A	00001778	4	853	1116
T11	A	00001838	4	888	1117
T12	A	000018F8	4	923	1118
T13	A	000019B8	4	961	1119

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T14	A	00001A78	4	996	1120
T15	A	00001B38	4	1031	1121
T16	A	00001BF8	4	1066	1122
T2	A	00001178	4	571	1108
T3	A	00001238	4	606	1109
T4	A	000012F8	4	641	1110
T5	A	000013B8	4	676	1111
T6	A	00001478	4	711	1112
T7	A	00001538	4	746	1113
T8	A	000015F8	4	781	1114
T9	A	000016B8	4	818	1115
TESTING	F	00001004	4	376	213
TNUM	H	00000004	2	414	212 260
TSUB	A	00000000	4	413	216
TTABLE	F	00001CBC	4	1106	
V0	U	00000000	1	1155	
V1	U	00000001	1	1156	215
V10	U	0000000A	1	1165	
V11	U	0000000B	1	1166	
V12	U	0000000C	1	1167	
V13	U	0000000D	1	1168	
V14	U	0000000E	1	1169	
V15	U	0000000F	1	1170	
V16	U	00000010	1	1171	
V17	U	00000011	1	1172	
V18	U	00000012	1	1173	
V19	U	00000013	1	1174	
V1FUDGE	X	00001094	16	405	215
V1O1	X	000010E8	16	547	558
V1O10	X	000017A8	16	864	875
V1O11	X	00001868	16	899	910
V1O12	X	00001928	16	934	945
V1O13	X	000019E8	16	972	983
V1O14	X	00001AA8	16	1007	1018
V1O15	X	00001B68	16	1042	1053
V1O16	X	00001C28	16	1077	1088
V1O2	X	000011A8	16	582	593
V1O3	X	00001268	16	617	628
V1O4	X	00001328	16	652	663
V1O5	X	000013E8	16	687	698
V1O6	X	000014A8	16	722	733
V1O7	X	00001568	16	757	768
V1O8	X	00001628	16	792	803
V1O9	X	000016E8	16	829	840
V1OUTPUT	X	00000030	16	425	220
V2	U	00000002	1	1157	
V20	U	00000014	1	1175	
V21	U	00000015	1	1176	
V22	U	00000016	1	1177	552 557 558 587 592 593 622 627 628 657 662 663 692 697 698 727 732 733 762 767 768 797 802 803 834 839 840 869 874 875 904 909 910 939 944 945 977 982 983 1012 1017 1018 1047 1052 1053 1082 1087 1088
V23	U	00000017	1	1178	554 557 589 592 624 627 659 662 694 697 729 732 764 767 799 802 836 839 871 874 906 909 941 944 979 982 1014 1017 1049 1052 1084 1087
V24	U	00000018	1	1179	556 557 591 592 626 627 661 662 696 697 731 732 766

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					767 801 802 838 839 873 874 908 909 943 944 981 982 1016 1017 1051 1052 1086 1087
V25	U	00000019	1	1180	
V26	U	0000001A	1	1181	
V27	U	0000001B	1	1182	
V28	U	0000001C	1	1183	
V29	U	0000001D	1	1184	
V2ADDR	A	00000010	4	419	551 586 621 656 691 726 761 796 833 868 903 938 976 1011 1046 1081
V3	U	00000003	1	1158	
V30	U	0000001E	1	1185	
V31	U	0000001F	1	1186	
V3ADDR	A	00000014	4	420	553 588 623 658 693 728 763 798 835 870 905 940 978 1013 1048 1083
V4	U	00000004	1	1159	
V4ADDR	A	00000018	4	421	555 590 625 660 695 730 765 800 837 872 907 942 980 1015 1050 1085
V5	U	00000005	1	1160	
V6	U	00000006	1	1161	
V7	U	00000007	1	1162	
V8	U	00000008	1	1163	
V9	U	00000009	1	1164	
X0001	U	000002A8	1	183	171 184
X1	F	00001100	4	550	536
X10	F	000017C0	4	867	853
X11	F	00001880	4	902	888
X12	F	00001940	4	937	923
X13	F	00001A00	4	975	961
X14	F	00001AC0	4	1010	996
X15	F	00001B80	4	1045	1031
X16	F	00001C40	4	1080	1066
X2	F	000011C0	4	585	571
X3	F	00001280	4	620	606
X4	F	00001340	4	655	641
X5	F	00001400	4	690	676
X6	F	000014C0	4	725	711
X7	F	00001580	4	760	746
X8	F	00001640	4	795	781
X9	F	00001700	4	832	818
XC0001	U	000002D0	1	197	189
ZVE7TST	J	00000000	7436	110	113 115 119 123 374 111
=A(E7TESTS)	A	00000498	4	352	203
=AL2(L'MSGMSG)	R	000004A2	2	355	302
=F'1'	F	0000049C	4	353	238
=F'64'	F	00000494	4	351	188
=H'0'	H	000004A0	2	354	297

```
 MACRO    DEFN  REFERENCES

FCHECK     63    170
PTTABLE   493   1105
VRR_D     444    533    568    603    638    673    708    743    778    815    850    885    920    958    993   1028   1063
```

```
   DESC      SYMBOL   SIZE      POS         ADDR

Entry: 0

Image       IMAGE    7436   0000-1D0B   0000-1D0B
  Region             7436   0000-1D0B   0000-1D0B
    CSECT   ZVE7TST  7436   0000-1D0B   0000-1D0B
```

```
   STMT                         FILE NAME
1     /home/tn529/sharedvfp/tests/zvector-e7-03-VGFMA.asm

** NO ERRORS FOUND **
```