```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                      2 ************************************************************************
                                                      3 *
                                                      4 *        Zvector E6 instruction tests for VRI-h encoded:
                                                      5 *
                                                      6 *        E649 VLIP    - VECTOR LOAD IMMEDIATE DECIMAL
                                                      7 *
                                                      8 *        James Wekel June 2024
                                                      9 ************************************************************************
                                                     10
                                                     11 ************************************************************************
                                                     12 *
                                                     13 *        basic instruction tests
                                                     14 *
                                                     15 ************************************************************************
                                                     16 *  This program tests proper functioning of the z/arch E6 VRI-h vector
                                                     17 *  load immediate decimal. Exceptions are not tested.
                                                     18 *
                                                     19 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                     20 *  obvious coding errors.  None of the tests are thorough.  They are
                                                     21 *  NOT designed to test all aspects of any of the instructions.
                                                     22 *
                                                     23 ************************************************************************
                                                     24 *
                                                     25 *    *Testcase zvector-e6-10-VLIP: VECTOR E6 VRI-h VLIP instruction
                                                     26 *    *
                                                     27 *    *   Zvector E6 tests for VRI-h encoded instruction:
                                                     28 *    *
                                                     29 *    *   E649 VLIP    - VECTOR LOAD IMMEDIATE DECIMAL
                                                     30 *    *
                                                     31 *    *   # ---------------------------------------------------------
                                                     32 *    *   #  This tests only the basic function of the instruction.
                                                     33 *    *   #  Exceptions are NOT tested.
                                                     34 *    *   # ---------------------------------------------------------
                                                     35 *    *
                                                     36 *    mainsize    2
                                                     37 *    numcpu      1
                                                     38 *    sysclear
                                                     39 *    archlvl     z/Arch
                                                     40 *
                                                     41 *    diag8cmd    enable    # (needed for messages to Hercules console)
                                                     42 *    loadcore    "zvector-e6-10-VLIP.core" 0x0
                                                     43 *    diag8cmd    disable   # (reset back to default)
                                                     44 *
                                                     45 *    *Done
                                                     46 ************************************************************************
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    48 ************************************************************************
                                                    49 *        FCHECK Macro - Is a Facility Bit set?
                                                    50 *
                                                    51 *        If the facility bit is NOT set, an message is issued and
                                                    52 *        the test is skipped.
                                                    53 *
                                                    54 *        Fcheck uses R0, R1 and R2
                                                    55 *
                                                    56 * eg.    FCHECK 134,'vector-packed-decimal'
                                                    57 ************************************************************************
                                                    58          MACRO
                                                    59          FCHECK &BITNO,&NOTSETMSG
                                                    60 .*                      &BITNO : facility bit number to check
                                                    61 .*                      &NOTSETMSG : 'facility name'
                                                    62          LCLA  &FBBYTE           Facility bit in Byte
                                                    63          LCLA  &FBBIT            Facility bit within Byte
                                                    64
                                                    65          LCLA  &L(8)
                                                    66 &L(1)    SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                                    67
                                                    68 &FBBYTE  SETA  &BITNO/8
                                                    69 &FBBIT   SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                                    70 .*       MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                                    71
                                                    72          B     X&SYSNDX
                                                    73 *                                       Fcheck data area
                                                    74 *                                       skip messgae
                                                    75 SKT&SYSNDX DC  C'          Skipping tests: '
                                                    76          DC    C&NOTSETMSG
                                                    77          DC    C' facility (bit &BITNO) is not installed.'
                                                    78 SKL&SYSNDX EQU *-SKT&SYSNDX
                                                    79 *                                       facility bits
                                                    80          DS    FD                       gap
                                                    81 FB&SYSNDX DS   4FD
                                                    82          DS    FD                       gap
                                                    83 *
                                                    84 X&SYSNDX EQU *
                                                    85          LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                                    86          STFLE FB&SYSNDX                get facility bits
                                                    87
                                                    88          XGR   R0,R0
                                                    89          IC    R0,FB&SYSNDX+&FBBYTE     get fbit byte
                                                    90          N     R0,=F'&FBBIT'            is bit set?
                                                    91          BNZ   XC&SYSNDX
                                                    92 *
                                                    93 * facility bit not set, issue message and exit
                                                    94 *
                                                    95          LA    R0,SKL&SYSNDX            message length
                                                    96          LA    R1,SKT&SYSNDX            message address
                                                    97          BAL   R2,MSG
                                                    98
                                                    99          B     EOJ
                                                   100 XC&SYSNDX EQU *
                                                   101          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    103 ********************************************************************************
                                                    104 *        Low core PSWs
                                                    105 ********************************************************************************


                             00000000  0000141F    107 ZVE6TST  START 0
00000000                     00000000                108          USING ZVE6TST,R0            Low core addressability
                                                     109
                             00000140  00000000    110 SVOLDPSW EQU   ZVE6TST+X'140'        z/Arch Supervisor call old PSW


00000000                     00000000  000001A0    112          ORG   ZVE6TST+X'1A0'       z/Architecure RESTART PSW
000001A0  00000001 80000000                         113          DC    X'0000000180000000'
000001A8  00000000 00000200                         114          DC    AD(BEGIN)


000001B0                     000001B0  000001D0    116          ORG   ZVE6TST+X'1D0'       z/Architecure PROGRAM CHECK PSW
000001D0  00020001 80000000                         117          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                         118          DC    AD(X'DEAD')


000001E0                     000001E0  00000200    120          ORG   ZVE6TST+X'200'       Start of actual test program...
                                                    121
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     123 ************************************************************************
                                                     124 *               The actual "ZVE6TST" program itself...
                                                     125 ************************************************************************
                                                     126 *
                                                     127 *  Architecture Mode: z/Arch
                                                     128 *  Register Usage:
                                                     129 *
                                                     130 *   R0       (work)
                                                     131 *   R1-4     (work)
                                                     132 *   R5       Testing control table - current test base
                                                     133 *   R6-R7    (work)
                                                     134 *   R8       First base register
                                                     135 *   R9       Second base register
                                                     136 *   R10      Third base register
                                                     137 *   R11      E6TEST call return
                                                     138 *   R12      E6TESTS register
                                                     139 *   R13      (work)
                                                     140 *   R14      Subroutine call
                                                     141 *   R15      Secondary Subroutine call or work
                                                     142 *
                                                     143 ************************************************************************

00000200                          00000200           145          USING  BEGIN,R8        FIRST Base Register
00000200                          00001200           146          USING  BEGIN+4096,R9   SECOND Base Register
00000200                          00002200           147          USING  BEGIN+8192,R10  THIRD Base Register
                                                     148
00000200  0580                                       149 BEGIN    BALR   R8,0            Initalize FIRST base register
00000202  0680                                       150          BCTR   R8,0            Initalize FIRST base register
00000204  0680                                       151          BCTR   R8,0            Initalize FIRST base register
                                                     152
00000206  4190 8800                      00000800    153          LA     R9,2048(,R8)    Initalize SECOND base register
0000020A  4190 9800                      00000800    154          LA     R9,2048(,R9)    Initalize SECOND base register
                                                     155
0000020E  41A0 9800                      00000800    156          LA     R10,2048(,R9)   Initalize THIRD base register
00000212  41A0 A800                      00000800    157          LA     R10,2048(,R10)  Initalize THIRD base register
                                                     158
00000216  B600 82B4                      000004B4    159          STCTL  R0,R0,CTLR0     Store CR0 to enable AFP
0000021A  9604 82B5                      000004B5    160          OI     CTLR0+1,X'04'   Turn on AFP bit
0000021E  9602 82B5                      000004B5    161          OI     CTLR0+1,X'02'   Turn on Vector bit
00000222  B700 82B4                      000004B4    162          LCTL   R0,R0,CTLR0     Reload updated CR0
                                                     163
                                                     164 ************************************************************************
                                                     165 * Is Vector packed-decimal facility installed  (bit 134)
                                                     166 ************************************************************************
                                                     167
                                                     168          FCHECK 134,'vector-packed-decimal'
00000226  47F0 80B0                      000002B0    169+         B      X0001
                                                     170+*                                  Fcheck data area
                                                     171+*                                  skip messgae
0000022A  40404040 40404040                          172+SKT0001  DC     C'          Skipping tests: '
00000244  A58583A3 96996097                          173+         DC     C'vector-packed-decimal'
00000259  40868183 899389A3                          174+         DC     C' facility (bit 134) is not installed.'
                            00000054  00000001       175+SKL0001  EQU    *-SKT0001
                                                     176+*                                  facility bits
00000280  00000000 00000000                          177+         DS     FD              gap
00000288  00000000 00000000                          178+FB0001   DS     4FD
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
000002A8  00000000 00000000                        179+          DS    FD                        gap
                                                   180+*
                             000002B0  00000001    181+X0001     EQU   *
000002B0  4100 0004                    00000004    182+          LA    R0,((X0001-FB0001)/8)-1
000002B4  B2B0 8088                    00000288    183+          STFLE FB0001                    get facility bits
000002B8  B982 0000                                184+          XGR   R0,R0
000002BC  4300 8098                    00000298    185+          IC    R0,FB0001+16              get fbit byte
000002C0  5400 82BC                    000004BC    186+          N     R0,=F'2'                  is bit set?
000002C4  4770 80D8                    000002D8    187+          BNZ   XC0001
                                                   188+*
                                                   189+* facility bit not set, issue message and exit
                                                   190+*
000002C8  4100 0054                    00000054    191+          LA    R0,SKL0001                message length
000002CC  4110 802A                    0000022A    192+          LA    R1,SKT0001                message address
000002D0  4520 81D0                    000003D0    193+          BAL   R2,MSG
000002D4  47F0 8298                    00000498    194+          B     EOJ
                             000002D8  00000001    195+XC0001    EQU   *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    197 ************************************************************************
                                                    198 *               Do tests in the E6TESTS table
                                                    199 ************************************************************************
                                                    200
000002D8  58C0 82C0                      000004C0   201           L     R12,=A(E6TESTS)       get table of test addresses
                                                    202
                                000002DC  00000001  203 NEXTE6    EQU   *
000002DC  5850 C000                      00000000   204           L     R5,0(0,R12)       get test address
000002E0  1255                                      205           LTR   R5,R5                have a test?
000002E2  4780 818A                      0000038A   206           BZ    ENDTEST                 done?
                                                    207
000002E6                        00000000            208           USING E6TEST,R5
                                                    209
000002E6  4800 5004                      00000004   210           LH    R0,TNUM             save current test number
000002EA  5000 8E04                      00001004   211           ST    R0,TESTING          for easy reference
                                                    212
000002EE  E710 8EE0 0006                 000010E0   213           VL    V1,V1FUDGEB         fudge output
                                                    214
000002F4  58B0 5000                      00000000   215           L     R11,TSUB            get address of test routine
000002F8  05BB                                      216           BALR  R11,R11             do test
                                                    217
                                000002FA  00000001  218 TESTREST  EQU   *
000002FA  E310 5018 0014                 00000018   219           LGF   R1,READDR           get address of expected result
00000300  D50F 8EB0 1000        000010B0 00000000   220           CLC   V1OUTPUT,0(R1)      valid?
00000306  4770 8112                      00000312   221           BNE   FAILMSG                needs, issue failed message
                                                    222
0000030A  41C0 C004                      00000004   223           LA    R12,4(0,R12)        next test address
0000030E  47F0 80DC                      000002DC   224           B     NEXTE6
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    226 ************************************************************************
                                                    227 * result not as expected:
                                                    228 *        issue message with test number, instruction under test
                                                    229 *              and instruction l2
                                                    230 ************************************************************************
                               00000312  00000001   231 FAILMSG  EQU   *
00000312  4820 5004                      00000004   232          LH    R2,TNUM              get test number and convert
00000316  4E20 8E82                      00001082   233          CVD   R2,DECNUM
0000031A  D211 8E6C 8E56       0000106C  00001056   234          MVC   PRT3,EDIT
00000320  DE11 8E6C 8E82       0000106C  00001082   235          ED    PRT3,DECNUM
00000326  D202 8E18 8E79       00001018  00001079   236          MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                    237
0000032C  D207 8E33 500A       00001033  0000000A   238          MVC   PRTNAME,OPNAME       fill in message with instruction
                                                    239
00000332  B982 0022                                 240          XGR   R2,R2                get i2 as U16
00000336  4820 5008                      00000008   241          LH    R2,I2
0000033A  4E20 8E82                      00001082   242          CVD   R2,DECNUM            and convert
0000033E  D211 8E6C 8E56       0000106C  00001056   243          MVC   PRT3,EDIT
00000344  DE11 8E6C 8E82       0000106C  00001082   244          ED    PRT3,DECNUM
0000034A  D204 8E44 8E77       00001044  00001077   245          MVC   PRTI2(5),PRT3+11     fill in message with i2 field
                                                    246
00000350  B982 0022                                 247          XGR   R2,R2                get i3 as U8
00000354  4320 5007                      00000007   248          IC    R2,I3                and convert
00000358  4E20 8E82                      00001082   249          CVD   R2,DECNUM
0000035C  D211 8E6C 8E56       0000106C  00001056   250          MVC   PRT3,EDIT
00000362  DE11 8E6C 8E82       0000106C  00001082   251          ED    PRT3,DECNUM
00000368  D201 8E53 8E7A       00001053  0000107A   252          MVC   PRTI3(2),PRT3+14     fill in message with i3 field
                                                    253
0000036E  4100 004E                      0000004E   254          LA    R0,PRTLNG            message length
00000372  4110 8E08                      00001008   255          LA    R1,PRTLINE           messagfe address
00000376  45F0 8198                      00000398   256          BAL   R15,RPTERROR


                                                    258 ************************************************************************
                                                    259 * continue after a failed test
                                                    260 ************************************************************************
                               0000037A  00000001   261 FAILCONT EQU   *
0000037A  5800 82C4                      000004C4   262          L     R0,=F'1'             set GLOBAL failed test indicator
0000037E  5000 8E00                      00001000   263          ST    R0,FAILED
                                                    264
00000382  41C0 C004                      00000004   265          LA    R12,4(0,R12)         next test address
00000386  47F0 80DC                      000002DC   266          B     NEXTE6


                                                    268 ************************************************************************
                                                    269 * end of testing; set ending psw
                                                    270 ************************************************************************
                               0000038A  00000001   271 ENDTEST  EQU   *
0000038A  5810 8E00                      00001000   272          L     R1,FAILED            did a test fail?
0000038E  1211                                      273          LTR   R1,R1
00000390  4780 8298                      00000498   274          BZ    EOJ                     No, exit
00000394  47F0 82B0                      000004B0   275          B     FAILTEST                Yes, exit with BAD PSW
                                                    276
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    278 ************************************************************************
                                                    279 *        RPTERROR          Report instruction test in error
                                                    280 *                             R0 = MESSGAE LENGTH
                                                    281 *                             R1 = ADDRESS OF MESSAGE
                                                    282 ************************************************************************

00000398  50F0 81B8                 000003B8    284 RPTERROR ST    R15,RPTSAVE        Save return address
0000039C  5050 81BC                 000003BC    285          ST    R5,RPTSVR5         Save R5
                                                    286 *
                                                    287 *        Use Hercules Diagnose for Message to console
                                                    288 *
000003A0  9002 81C0                 000003C0    289          STM   R0,R2,RPTDWSAV     save regs used by MSG
000003A4  4520 81D0                 000003D0    290          BAL   R2,MSG             call Hercules console MSG display
000003A8  9802 81C0                 000003C0    291          LM    R0,R2,RPTDWSAV     restore regs


000003AC  5850 81BC                 000003BC    293          L     R5,RPTSVR5         Restore R5
000003B0  58F0 81B8                 000003B8    294          L     R15,RPTSAVE        Restore return address
000003B4  07FF                                  295          BR    R15                Return to caller

000003B8  00000000                              297 RPTSAVE  DC    F'0'               R15 save area
000003BC  00000000                              298 RPTSVR5  DC    F'0'               R5 save area

000003C0  00000000 00000000                     300 RPTDWSAV DC    2D'0'              R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    302 ***************************************************************************
                                                    303 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                    304 *              R2 = return address
                                                    305 ***************************************************************************
                                                    306
000003D0  4900 82C8                    000004C8    307 MSG      CH    R0,=H'0'                Do we even HAVE a message?
000003D4  07D2                                     308          BNHR  R2                      No, ignore
                                                    309
000003D6  9002 820C                    0000040C    310          STM   R0,R2,MSGSAVE           Save registers
                                                    311
000003DA  4900 82CA                    000004CA    312          CH    R0,=AL2(L'MSGMSG)       Message length within limits?
000003DE  47D0 81E6                    000003E6    313          BNH   MSGOK                   Yes, continue
000003E2  4100 005F                    0000005F    314          LA    R0,L'MSGMSG             No, set to maximum
                                                    315
000003E6  1820                                     316 MSGOK    LR    R2,R0                   Copy length to work register
000003E8  0620                                     317          BCTR  R2,0                    Minus-1 for execute
000003EA  4420 8218                    00000418    318          EX    R2,MSGMVC               Copy message to O/P buffer
                                                    319
000003EE  4120 200A                    0000000A    320          LA    R2,1+L'MSGCMD(,R2)      Calculate true command length
000003F2  4110 821E                    0000041E    321          LA    R1,MSGCMD               Point to true command
                                                    322
000003F6  83120008                                 323          DC    X'83',X'12',X'0008'     Issue Hercules Diagnose X'008'
000003FA  4780 8206                    00000406    324          BZ    MSGRET                  Return if successful
                                                    325
000003FE  1222                                     326          LTR   R2,R2                   Is Diag8 Ry (R2) 0?
00000400  4780 8206                    00000406    327          BZ    MSGRET                    an error occurred but coninue
                                                    328
00000404  0000                                     329          DC    H'0'                    CRASH for debugging purposes
                                                    330
00000406  9802 820C                    0000040C    331 MSGRET   LM    R0,R2,MSGSAVE           Restore registers
0000040A  07F2                                     332          BR    R2                      Return to caller


0000040C  00000000 00000000                        334 MSGSAVE  DC    3F'0'                   Registers save area
00000418  D200 8227 1000      00000427 00000000    335 MSGMVC   MVC   MSGMSG(0),0(R1)          Executed instruction

0000041E  D4E2C7D5 D6C8405C                        337 MSGCMD   DC    C'MSGNOH * '            *** HERCULES MESSAGE COMMAND ***
00000427  40404040 40404040                        338 MSGMSG   DC    CL95' '                 The message text to be displayed
                                                    339
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      341 ************************************************************************
                                                      342 *        Normal completion or Abnormal termination PSWs
                                                      343 ************************************************************************


00000488  00020001 80000000                           345 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)

00000498  B2B2 8288                   00000488        347 EOJ      LPSWE EOJPSW               Normal completion


000004A0  00020001 80000000                           349 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')

000004B0  B2B2 82A0                   000004A0        351 FAILTEST LPSWE FAILPSW              Abnormal termination


                                                      353 ************************************************************************
                                                      354 *        Working Storage
                                                      355 ************************************************************************

000004B4  00000000                                    357 CTLR0    DS    F                    CR0
000004B8  00000000                                    358          DS    F


000004BC                                              360          LTORG ,                    Literals pool
000004BC  00000002                                    361                =F'2'
000004C0  000013E4                                    362                =A(E6TESTS)
000004C4  00000001                                    363                =F'1'
000004C8  0000                                        364                =H'0'
000004CA  005F                                        365                =AL2(L'MSGMSG)
                                                      366
                                                      367 *        some constants
                                                      368
                          00000400  00000001          369 K        EQU   1024                 One KB
                          00001000  00000001          370 PAGE     EQU   (4*K)                Size of one page
                          00010000  00000001          371 K64      EQU   (64*K)               64 KB
                          00100000  00000001          372 MB       EQU   (K*K)                 1 MB
                                                      373
                          AABBCCDD  00000001          374 REG2PATT EQU   X'AABBCCDD'     Polluted Register pattern
                          000000DD  00000001          375 REG2LOW  EQU         X'DD'     (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     377 *=====================================================================
                                                     378 *
                                                     379 *  NOTE: start data on an address that is easy to display
                                                     380 *        within Hercules
                                                     381 *
                                                     382 *=====================================================================
                                                     383
000004CC                      000004CC  00001000     384          ORG   ZVE6TST+X'1000'
00001000  00000000                                   385 FAILED   DC    F'0'                    some test failed?
00001004  00000000                                   386 TESTING  DC    F'0'                    current test number

                                                     388 ************************************************************************
                                                     389 *        TEST failed : result messgae
                                                     390 ************************************************************************
                                                     391 *
                                                     392 *        failed message and associated editting
                                                     393 *
00001008  40404040 40404040                          394 PRTLINE  DC    C'         Test # '
00001018  A7A7A7                                     395 PRTNUM   DC    C'xxx'
0000101B  40868189 93858440                          396          DC    C' failed for instruction '
00001033  A7A7A7A7 A7A7A7A7                          397 PRTNAME  DC    CL8'xxxxxxxx'
0000103B  40A689A3 884089F2                          398          DC    C' with i2='
00001044  A7A7A7A7 A7                                399 PRTI2    DC    C'xxxxx'
00001049  6B                                         400          DC    C','
0000104A  40A689A3 884089F3                          401          DC    C' with i3='
00001053  A7A7                                       402 PRTI3    DC    C'xx'
00001055  4B                                         403          DC    C'.'
                                0000004E  00000001   404 PRTLNG   EQU   *-PRTLINE
                                                     405
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     407 ************************************************************************
                                                     408 *        TEST failed : message working storge
                                                     409 ************************************************************************
00001056  40212020 20202020                          410 EDIT     DC    XL18'4021202020202020202020202020202020'
                                                     411
00001068  7E7E7E6E                                   412          DC    C'===>'
0000106C  40404040 40404040                          413 PRT3     DC    CL18' '
0000107E  4C7E7E7E                                   414          DC    C'<==='
00001082  00000000 00000000                          415 DECNUM   DS    CL16
                                                     416 *
                                                     417 *        CC extrtaction
                                                     418 *
00001094  00000000 00000000                          419 CCPSW    DS    2F          extract PSW after test (has CC)
0000109C  00                                         420 CCFOUND  DS    X           extracted cc


                                                     422 ************************************************************************
                                                     423 *        Vector instruction results, pollution and input
                                                     424 ************************************************************************
000010A0                                             425          DS    0FD
000010A0  00000000 00000000                          426          DS    XL16                                          gap
000010B0  00000000 00000000                          427 V1OUTPUT DS    XL16                                       V1 OUTPUT
000010C0  00000000 00000000                          428          DS    XL16                                          gap
000010D0  FFFFFFFF FFFFFFFF                          429 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
000010E0  BBBBBBBB BBBBBBBB                          430 V1FUDGEB DC    XL16'BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB'    V1 FUDGE b
000010F0  F1F2F3F4 F5F6F7F8                          431 V1INPUT  DC    CL16'1234567890123456'                    V1 input
00001100  F7F8F9F0 F1F2F3F4                          432          DC    CL14'78901234567890'
0000110E  D9                                         433          DC    X'D9'
0000110F  00000000 00000000                          434          DS    XL16                                          gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                     436 ********************************************************************************
                                                     437 *        E6TEST DSECT
                                                     438 ********************************************************************************


                                                     440 E6TEST   DSECT ,
00000000  00000000                                   441 TSUB     DC    A(0)           pointer  to test
00000004  0000                                       442 TNUM     DC    H'00'          Test Number
00000006  00                                         443          DC    XL1'00'
00000007  00                                         444 I3       DC    HL1'00'        I3
00000008  0000                                       445 I2       DC    H'00'          I2 used
                                                     446
0000000A  40404040 40404040                          447 OPNAME   DC    CL8' '         E6 name
                                                     448
00000014  00000000                                   449 RELEN    DC    A(0)           RESULT LENGTH
00000018  00000000                                   450 READDR   DC    A(0)           expected result address
                                                     451
                                                     452 **
                                                     453 *        test routine will be here (from VRS_D macro)
                                                     454 * followed by
                                                     455 *        16-byte EXPECTED RESULT
                                                     456 *        16-byte source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     458 ************************************************************************
                                                     459 *     Macros to help build test tables
                                                     460 *----------------------------------------------------------------------
                                                     461 *     VRI_H Macro to help build test tables
                                                     462 ************************************************************************
                                                     463          MACRO
                                                     464          VRI_H &INST,&I2,&I3
                                                     465 .*                                  &INST  - VRS-d instruction under test
                                                     466 .*                                  &I2    - 4 decimal immediate (2 bytes)
                                                     467 .*                                  &I3    - bit 0   Sign Control
                                                     468 .*                                         - bit 1-3 Shift Amount
                                                     469 .*
                                                     470 .*
                                                     471          LCLA  &XCC(4)  &CC has mask values for FAILED condition codes
                                                     472 &XCC(1)  SETA  7                  CC != 0
                                                     473 &XCC(2)  SETA  11                 CC != 1
                                                     474 &XCC(3)  SETA  13                 CC != 2
                                                     475 &XCC(4)  SETA  14                 CC != 3
                                                     476
                                                     477          GBLA  &TNUM
                                                     478 &TNUM    SETA  &TNUM+1
                                                     479
                                                     480          DS    0FD
                                                     481          USING *,R5              base for test data and test routine
                                                     482
                                                     483 T&TNUM   DC    A(X&TNUM)         address of test routine
                                                     484          DC    H'&TNUM'          test number
                                                     485          DC    XL1'00'
                                                     486          DC    HL1'&I3'          i3
                                                     487          DC    H'&I2'            i2
                                                     488
                                                     489          DC    CL8'&INST'        instruction name
                                                     490
                                                     491          DC    A(16)             result length
                                                     492 REA&TNUM DC    A(RE&TNUM)        result address
                                                     493 .*
                                                     494 *                                INSTRUCTION UNDER TEST ROUTINE
                                                     495 X&TNUM   DS    0F
                                                     496          &INST V1,&I2,&I3        test instruction
                                                     497          VST   V1,V1OUTPUT       save
                                                     498
                                                     499          BR    R11               return
                                                     500
                                                     501 RE&TNUM  DC    0F
                                                     502          DROP  R5
                                                     503          MEND
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                      505 ********************************************************************************
                                                      506 *     PTTABLE Macro to generate table of pointers to individual tests
                                                      507 ********************************************************************************
                                                      508
                                                      509          MACRO
                                                      510          PTTABLE
                                                      511          GBLA  &TNUM
                                                      512          LCLA  &CUR
                                                      513 &CUR     SETA  1
                                                      514 .*
                                                      515 TTABLE   DS    0F
                                                      516 .LOOP    ANOP
                                                      517 .*
                                                      518          DC    A(T&CUR)           address of test
                                                      519 .*
                                                      520 &CUR     SETA  &CUR+1
                                                      521          AIF   (&CUR LE &TNUM).LOOP
                                                      522 *
                                                      523          DC    A(0)               END OF TABLE
                                                      524          DC    A(0)
                                                      525 .*
                                                      526          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     528 ********************************************************************************
                                                     529 *        E6 VRI_H tests
                                                     530 ********************************************************************************
                                00000000  0000141F   531 ZVE6TST  CSECT ,
00001120                                             532          DS    0F


                                                     534          PRINT DATA
                                                     535 *
                                                     536 *        E649 VLIP    - VECTOR LOAD IMMEDIATE DECIMAL
                                                     537 *
                                                     538 *        VRI_H instr, i2, i3
                                                     539 *             followed by
                                                     540 *             v1     - 16 byte expected result
                                                     541
                                                     542 *-------------------------------------------------------------------
                                                     543 * VLIP    - VECTOR LOAD IMMEDIATE DECIMAL
                                                     544 *-------------------------------------------------------------------
                                                     545 * VLIP simple
                                                     546          VRI_H VLIP,22102,2                 i2=x'5656' sc=0, shamt=2
00001120                                             547+         DS    0FD
00001120                                00001120     548+         USING *,R5              base for test data and test routine
00001120  0000113C                                   549+T1       DC    A(X1)             address of test routine
00001124  0001                                       550+         DC    H'1'              test number
00001126  00                                         551+         DC    XL1'00'
00001127  02                                         552+         DC    HL1'2'            i3
00001128  5656                                       553+         DC    H'22102'          i2
0000112A  E5D3C9D7 40404040                          554+         DC    CL8'VLIP'         instruction name
00001134  00000010                                   555+         DC    A(16)             result length
00001138  0000114C                                   556+REA1     DC    A(RE1)            result address
                                                     557+*                                  INSTRUCTION UNDER TEST ROUTINE
0000113C                                             558+X1       DS    0F
0000113C  E610 5656 2049                             559+         VLIP  V1,22102,2        test instruction
00001142  E710 8EB0 000E                 000010B0    560+         VST   V1,V1OUTPUT       save
00001148  07FB                                       561+         BR    R11               return
0000114C                                             562+RE1      DC    0F
0000114C                                             563+         DROP  R5
0000114C  00000000 00000000                          564          DC    XL16'00000000000000000000000000565600C'   V1
00001154  00000000 0565600C
                                                     565
                                                     566          VRI_H VLIP,22102,10                i2=x'5656' sc=1, shamt=2
00001160                                             567+         DS    0FD
00001160                         00001160            568+         USING *,R5              base for test data and test routine
00001160  0000117C                                   569+T2       DC    A(X2)             address of test routine
00001164  0002                                       570+         DC    H'2'              test number
00001166  00                                         571+         DC    XL1'00'
00001167  0A                                         572+         DC    HL1'10'           i3
00001168  5656                                       573+         DC    H'22102'          i2
0000116A  E5D3C9D7 40404040                          574+         DC    CL8'VLIP'         instruction name
00001174  00000010                                   575+         DC    A(16)             result length
00001178  0000118C                                   576+REA2     DC    A(RE2)            result address
                                                     577+*                                  INSTRUCTION UNDER TEST ROUTINE
0000117C                                             578+X2       DS    0F
0000117C  E610 5656 A049                             579+         VLIP  V1,22102,10       test instruction
00001182  E710 8EB0 000E                 000010B0    580+         VST   V1,V1OUTPUT       save
00001188  07FB                                       581+         BR    R11               return
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000118C                                          582+RE2      DC    0F
0000118C                                          583+         DROP  R5
0000118C  00000000 00000000                       584          DC    XL16'0000000000000000000000000565600D'   V1
00001194  00000000 0565600D
                                                  585
                                                  586          VRI_H VLIP,22102,7                 i2=x'5656' sc=0, shamt=7
000011A0                                          587+         DS    0FD
000011A0                        000011A0          588+         USING *,R5               base for test data and test routine
000011A0  000011BC                                589+T3       DC    A(X3)              address of test routine
000011A4  0003                                    590+         DC    H'3'               test number
000011A6  00                                      591+         DC    XL1'00'
000011A7  07                                      592+         DC    HL1'7'             i3
000011A8  5656                                    593+         DC    H'22102'           i2
000011AA  E5D3C9D7 40404040                       594+         DC    CL8'VLIP'          instruction name
000011B4  00000010                                595+         DC    A(16)              result length
000011B8  000011CC                                596+REA3     DC    A(RE3)             result address
                                                  597+*                                 INSTRUCTION UNDER TEST ROUTINE
000011BC                                          598+X3       DS    0F
000011BC  E610 5656 7049                          599+         VLIP  V1,22102,7         test instruction
000011C2  E710 8EB0 000E                000010B0  600+         VST   V1,V1OUTPUT        save
000011C8  07FB                                    601+         BR    R11                return
000011CC                                          602+RE3      DC    0F
000011CC                                          603+         DROP  R5
000011CC  00000000 00000000                       604          DC    XL16'0000000000000000000056560000000C'   V1
000011D4  00005656 0000000C
                                                  605
                                                  606          VRI_H VLIP,1,8                     i2=x'0001' sc=1, shamt=0
000011E0                                          607+         DS    0FD
000011E0                        000011E0          608+         USING *,R5               base for test data and test routine
000011E0  000011FC                                609+T4       DC    A(X4)              address of test routine
000011E4  0004                                    610+         DC    H'4'               test number
000011E6  00                                      611+         DC    XL1'00'
000011E7  08                                      612+         DC    HL1'8'             i3
000011E8  0001                                    613+         DC    H'1'               i2
000011EA  E5D3C9D7 40404040                       614+         DC    CL8'VLIP'          instruction name
000011F4  00000010                                615+         DC    A(16)              result length
000011F8  0000120C                                616+REA4     DC    A(RE4)             result address
                                                  617+*                                 INSTRUCTION UNDER TEST ROUTINE
000011FC                                          618+X4       DS    0F
000011FC  E610 0001 8049                          619+         VLIP  V1,1,8             test instruction
00001202  E710 8EB0 000E                000010B0  620+         VST   V1,V1OUTPUT        save
00001208  07FB                                    621+         BR    R11                return
0000120C                                          622+RE4      DC    0F
0000120C                                          623+         DROP  R5
0000120C  00000000 00000000                       624          DC    XL16'0000000000000000000000000000001D'   V1
00001214  00000000 0000001D
                                                  625
                                                  626          VRI_H VLIP,0,8                     i2=x'0001' sc=1, shamt=0
00001220                                          627+         DS    0FD
00001220                        00001220          628+         USING *,R5               base for test data and test routine
00001220  0000123C                                629+T5       DC    A(X5)              address of test routine
00001224  0005                                    630+         DC    H'5'               test number
00001226  00                                      631+         DC    XL1'00'
00001227  08                                      632+         DC    HL1'8'             i3
00001228  0000                                    633+         DC    H'0'               i2
0000122A  E5D3C9D7 40404040                       634+         DC    CL8'VLIP'          instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001234  00000010                                635+         DC    A(16)             result length
00001238  0000124C                                636+REA5     DC    A(RE5)            result address
                                                  637+*                                  INSTRUCTION UNDER TEST ROUTINE
0000123C                                          638+X5       DS    0F
0000123C  E610 0000 8049                          639+         VLIP  V1,0,8            test instruction
00001242  E710 8EB0 000E              000010B0    640+         VST   V1,V1OUTPUT       save
00001248  07FB                                    641+         BR    R11               return
0000124C                                          642+RE5      DC    0F
0000124C                                          643+         DROP  R5
0000124C  00000000 00000000                       644          DC    XL16'0000000000000000000000000000000D'   V1
00001254  00000000 0000000D
                                                  645
                                                  646          VRI_H VLIP,9,0                    i2=x'0009' sc=0, shamt=0
00001260                                          647+         DS    0FD
00001260                      00001260            648+         USING *,R5              base for test data and test routine
00001260  0000127C                                649+T6       DC    A(X6)             address of test routine
00001264  0006                                    650+         DC    H'6'              test number
00001266  00                                      651+         DC    XL1'00'
00001267  00                                      652+         DC    HL1'0'            i3
00001268  0009                                    653+         DC    H'9'              i2
0000126A  E5D3C9D7 40404040                       654+         DC    CL8'VLIP'         instruction name
00001274  00000010                                655+         DC    A(16)             result length
00001278  0000128C                                656+REA6     DC    A(RE6)            result address
                                                  657+*                                  INSTRUCTION UNDER TEST ROUTINE
0000127C                                          658+X6       DS    0F
0000127C  E610 0009 0049                          659+         VLIP  V1,9,0            test instruction
00001282  E710 8EB0 000E              000010B0    660+         VST   V1,V1OUTPUT       save
00001288  07FB                                    661+         BR    R11               return
0000128C                                          662+RE6      DC    0F
0000128C                                          663+         DROP  R5
0000128C  00000000 00000000                       664          DC    XL16'0000000000000000000000000000009C'   V1
00001294  00000000 0000009C
                                                  665
                                                  666          VRI_H VLIP,9,1                    i2=x'0009' sc=0, shamt=1
000012A0                                          667+         DS    0FD
000012A0                      000012A0            668+         USING *,R5              base for test data and test routine
000012A0  000012BC                                669+T7       DC    A(X7)             address of test routine
000012A4  0007                                    670+         DC    H'7'              test number
000012A6  00                                      671+         DC    XL1'00'
000012A7  01                                      672+         DC    HL1'1'            i3
000012A8  0009                                    673+         DC    H'9'              i2
000012AA  E5D3C9D7 40404040                       674+         DC    CL8'VLIP'         instruction name
000012B4  00000010                                675+         DC    A(16)             result length
000012B8  000012CC                                676+REA7     DC    A(RE7)            result address
                                                  677+*                                  INSTRUCTION UNDER TEST ROUTINE
000012BC                                          678+X7       DS    0F
000012BC  E610 0009 1049                          679+         VLIP  V1,9,1            test instruction
000012C2  E710 8EB0 000E              000010B0    680+         VST   V1,V1OUTPUT       save
000012C8  07FB                                    681+         BR    R11               return
000012CC                                          682+RE7      DC    0F
000012CC                                          683+         DROP  R5
000012CC  00000000 00000000                       684          DC    XL16'0000000000000000000000000000090C'   V1
000012D4  00000000 0000090C
                                                  685
                                                  686          VRI_H VLIP,4660,0                 i2=x'1234' sc=0, shamt=0
000012E0                                          687+         DS    0FD
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000012E0                      000012E0              688+         USING *,R5              base for test data and test routine
000012E0  000012FC                                  689+T8       DC    A(X8)             address of test routine
000012E4  0008                                      690+         DC    H'8'              test number
000012E6  00                                        691+         DC    XL1'00'
000012E7  00                                        692+         DC    HL1'0'            i3
000012E8  1234                                      693+         DC    H'4660'           i2
000012EA  E5D3C9D7 40404040                         694+         DC    CL8'VLIP'         instruction name
000012F4  00000010                                  695+         DC    A(16)             result length
000012F8  0000130C                                  696+REA8     DC    A(RE8)            result address
                                                    697+*                                INSTRUCTION UNDER TEST ROUTINE
000012FC                                            698+X8       DS    0F
000012FC  E610 1234 0049                            699+         VLIP  V1,4660,0         test instruction
00001302  E710 8EB0 000E              000010B0      700+         VST   V1,V1OUTPUT       save
00001308  07FB                                      701+         BR    R11               return
0000130C                                            702+RE8      DC    0F
0000130C                                            703+         DROP  R5
0000130C  00000000 00000000                         704          DC    XL16'00000000000000000000000001234C'   V1
00001314  00000000 0001234C
                                                    705
                                                    706          VRI_H VLIP,4660,1                  i2=x'1234' sc=0, shamt=1
00001320                                            707+         DS    0FD
00001320                      00001320              708+         USING *,R5              base for test data and test routine
00001320  0000133C                                  709+T9       DC    A(X9)             address of test routine
00001324  0009                                      710+         DC    H'9'              test number
00001326  00                                        711+         DC    XL1'00'
00001327  01                                        712+         DC    HL1'1'            i3
00001328  1234                                      713+         DC    H'4660'           i2
0000132A  E5D3C9D7 40404040                         714+         DC    CL8'VLIP'         instruction name
00001334  00000010                                  715+         DC    A(16)             result length
00001338  0000134C                                  716+REA9     DC    A(RE9)            result address
                                                    717+*                                INSTRUCTION UNDER TEST ROUTINE
0000133C                                            718+X9       DS    0F
0000133C  E610 1234 1049                            719+         VLIP  V1,4660,1         test instruction
00001342  E710 8EB0 000E              000010B0      720+         VST   V1,V1OUTPUT       save
00001348  07FB                                      721+         BR    R11               return
0000134C                                            722+RE9      DC    0F
0000134C                                            723+         DROP  R5
0000134C  00000000 00000000                         724          DC    XL16'00000000000000000000000012340C'   V1
00001354  00000000 0012340C
                                                    725
                                                    726          VRI_H VLIP,4660,2                  i2=x'1234' sc=0, shamt=2
00001360                                            727+         DS    0FD
00001360                      00001360              728+         USING *,R5              base for test data and test routine
00001360  0000137C                                  729+T10      DC    A(X10)            address of test routine
00001364  000A                                      730+         DC    H'10'             test number
00001366  00                                        731+         DC    XL1'00'
00001367  02                                        732+         DC    HL1'2'            i3
00001368  1234                                      733+         DC    H'4660'           i2
0000136A  E5D3C9D7 40404040                         734+         DC    CL8'VLIP'         instruction name
00001374  00000010                                  735+         DC    A(16)             result length
00001378  0000138C                                  736+REA10    DC    A(RE10)           result address
                                                    737+*                                INSTRUCTION UNDER TEST ROUTINE
0000137C                                            738+X10      DS    0F
0000137C  E610 1234 2049                            739+         VLIP  V1,4660,2         test instruction
00001382  E710 8EB0 000E              000010B0      740+         VST   V1,V1OUTPUT       save
00001388  07FB                                      741+         BR    R11               return
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
0000138C                                          742+RE10     DC    0F
0000138C                                          743+         DROP  R5
0000138C  00000000 00000000                       744          DC    XL16'0000000000000000000000000123400C'   V1
00001394  00000000 0123400C
                                                  745
                                                  746          VRI_H VLIP,4660,11                i2=x'1234' sc=1, shamt=3
000013A0                                          747+         DS    0FD
000013A0                          000013A0        748+         USING *,R5              base for test data and test routine
000013A0  000013BC                                749+T11      DC    A(X11)            address of test routine
000013A4  000B                                    750+         DC    H'11'             test number
000013A6  00                                      751+         DC    XL1'00'
000013A7  0B                                      752+         DC    HL1'11'           i3
000013A8  1234                                    753+         DC    H'4660'           i2
000013AA  E5D3C9D7 40404040                       754+         DC    CL8'VLIP'         instruction name
000013B4  00000010                                755+         DC    A(16)             result length
000013B8  000013CC                                756+REA11    DC    A(RE11)           result address
                                                  757+*                                INSTRUCTION UNDER TEST ROUTINE
000013BC                                          758+X11      DS    0F
000013BC  E610 1234 B049                          759+         VLIP  V1,4660,11        test instruction
000013C2  E710 8EB0 000E                000010B0  760+         VST   V1,V1OUTPUT       save
000013C8  07FB                                    761+         BR    R11               return
000013CC                                          762+RE11     DC    0F
000013CC                                          763+         DROP  R5
000013CC  00000000 00000000                       764          DC    XL16'0000000000000000000000001234000D'   V1
000013D4  00000000 1234000D
                                                  765
                                                  766
000013DC  00000000                                767          DC    F'0'     END OF TABLE
000013E0  00000000                                768          DC    F'0'
                                                  769 *
                                                  770 * table of pointers to individual load test
                                                  771 *
000013E4                                          772 E6TESTS  DS    0F
                                                  773          PTTABLE
000013E4                                          774+TTABLE   DS    0F
000013E4  00001120                                775+         DC    A(T1)             address of test
000013E8  00001160                                776+         DC    A(T2)             address of test
000013EC  000011A0                                777+         DC    A(T3)             address of test
000013F0  000011E0                                778+         DC    A(T4)             address of test
000013F4  00001220                                779+         DC    A(T5)             address of test
000013F8  00001260                                780+         DC    A(T6)             address of test
000013FC  000012A0                                781+         DC    A(T7)             address of test
00001400  000012E0                                782+         DC    A(T8)             address of test
00001404  00001320                                783+         DC    A(T9)             address of test
00001408  00001360                                784+         DC    A(T10)            address of test
0000140C  000013A0                                785+         DC    A(T11)            address of test
                                                  786+*
00001410  00000000                                787+         DC    A(0)              END OF TABLE
00001414  00000000                                788+         DC    A(0)
                                                  789
00001418  00000000                                790          DC    F'0'     END OF TABLE
0000141C  00000000                                791          DC    F'0'
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      793 ********************************************************************************
                                                      794 *        Register equates
                                                      795 ********************************************************************************

                                00000000  00000001    797 R0       EQU   0
                                00000001  00000001    798 R1       EQU   1
                                00000002  00000001    799 R2       EQU   2
                                00000003  00000001    800 R3       EQU   3
                                00000004  00000001    801 R4       EQU   4
                                00000005  00000001    802 R5       EQU   5
                                00000006  00000001    803 R6       EQU   6
                                00000007  00000001    804 R7       EQU   7
                                00000008  00000001    805 R8       EQU   8
                                00000009  00000001    806 R9       EQU   9
                                0000000A  00000001    807 R10      EQU   10
                                0000000B  00000001    808 R11      EQU   11
                                0000000C  00000001    809 R12      EQU   12
                                0000000D  00000001    810 R13      EQU   13
                                0000000E  00000001    811 R14      EQU   14
                                0000000F  00000001    812 R15      EQU   15

                                                      814 ********************************************************************************
                                                      815 *        Register equates
                                                      816 ********************************************************************************

                                00000000  00000001    818 V0       EQU   0
                                00000001  00000001    819 V1       EQU   1
                                00000002  00000001    820 V2       EQU   2
                                00000003  00000001    821 V3       EQU   3
                                00000004  00000001    822 V4       EQU   4
                                00000005  00000001    823 V5       EQU   5
                                00000006  00000001    824 V6       EQU   6
                                00000007  00000001    825 V7       EQU   7
                                00000008  00000001    826 V8       EQU   8
                                00000009  00000001    827 V9       EQU   9
                                0000000A  00000001    828 V10      EQU   10
                                0000000B  00000001    829 V11      EQU   11
                                0000000C  00000001    830 V12      EQU   12
                                0000000D  00000001    831 V13      EQU   13
                                0000000E  00000001    832 V14      EQU   14
                                0000000F  00000001    833 V15      EQU   15
                                00000010  00000001    834 V16      EQU   16
                                00000011  00000001    835 V17      EQU   17
                                00000012  00000001    836 V18      EQU   18
                                00000013  00000001    837 V19      EQU   19
                                00000014  00000001    838 V20      EQU   20
                                00000015  00000001    839 V21      EQU   21
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                00000016  00000001   840 V22      EQU   22
                                00000017  00000001   841 V23      EQU   23
                                00000018  00000001   842 V24      EQU   24
                                00000019  00000001   843 V25      EQU   25
                                0000001A  00000001   844 V26      EQU   26
                                0000001B  00000001   845 V27      EQU   27
                                0000001C  00000001   846 V28      EQU   28
                                0000001D  00000001   847 V29      EQU   29
                                0000001E  00000001   848 V30      EQU   30
                                0000001F  00000001   849 V31      EQU   31
                                                     850
                                                     851          END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
BEGIN	I	00000200	2	149	114 145 146 147
CCFOUND	X	0000109C	1	420	
CCPSW	F	00001094	4	419	
CTLR0	F	000004B4	4	357	159 160 161 162
DECNUM	C	00001082	16	415	233 235 242 244 249 251
E6TEST	4	00000000	28	440	208
E6TESTS	F	000013E4	4	772	201
EDIT	X	00001056	18	410	234 243 250
ENDTEST	U	0000038A	1	271	206
EOJ	I	00000498	4	347	194 274
EOJPSW	D	00000488	8	345	347
FAILCONT	U	0000037A	1	261	
FAILED	F	00001000	4	385	263 272
FAILMSG	U	00000312	1	231	221
FAILPSW	D	000004A0	8	349	351
FAILTEST	I	000004B0	4	351	275
FB0001	F	00000288	8	178	182 183 185
I2	H	00000008	2	445	241
I3	U	00000007	1	444	248
IMAGE	1	00000000	5152	0	
K	U	00000400	1	369	370 371 372
K64	U	00010000	1	371	
MB	U	00100000	1	372	
MSG	I	000003D0	4	307	193 290
MSGCMD	C	0000041E	9	337	320 321
MSGMSG	C	00000427	95	338	314 335 312
MSGMVC	I	00000418	6	335	318
MSGOK	I	000003E6	2	316	313
MSGRET	I	00000406	4	331	324 327
MSGSAVE	F	0000040C	4	334	310 331
NEXTE6	U	000002DC	1	203	224 266
OPNAME	C	0000000A	8	447	238
PAGE	U	00001000	1	370	
PRT3	C	0000106C	18	413	234 235 236 243 244 245 250 251 252
PRTI2	C	00001044	5	399	245
PRTI3	C	00001053	2	402	252
PRTLINE	C	00001008	16	394	404 255
PRTLNG	U	0000004E	1	404	254
PRTNAME	C	00001033	8	397	238
PRTNUM	C	00001018	3	395	236
R0	U	00000000	1	797	108 159 162 182 184 185 186 191 210 211 254 262 263 289 291
					307 310 312 314 316 331
R1	U	00000001	1	798	192 219 220 255 272 273 321 335
R10	U	0000000A	1	807	147 156 157
R11	U	0000000B	1	808	215 216 561 581 601 621 641 661 681 701 721 741 761
R12	U	0000000C	1	809	201 204 223 265
R13	U	0000000D	1	810	
R14	U	0000000E	1	811	
R15	U	0000000F	1	812	256 284 294 295
R2	U	00000002	1	799	193 232 233 240 241 242 247 248 249 289 290 291 308 310 316
					317 318 320 326 331 332
R3	U	00000003	1	800	
R4	U	00000004	1	801	
R5	U	00000005	1	802	204 205 208 285 293 548 563 568 583 588 603 608 623 628 643
					648 663 668 683 688 703 708 723 728 743 748 763
R6	U	00000006	1	803	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
R7	U	00000007	1	804	
R8	U	00000008	1	805	145 149 150 151 153
R9	U	00000009	1	806	146 153 154 156
RE1	F	0000114C	4	562	556
RE10	F	0000138C	4	742	736
RE11	F	000013CC	4	762	756
RE2	F	0000118C	4	582	576
RE3	F	000011CC	4	602	596
RE4	F	0000120C	4	622	616
RE5	F	0000124C	4	642	636
RE6	F	0000128C	4	662	656
RE7	F	000012CC	4	682	676
RE8	F	0000130C	4	702	696
RE9	F	0000134C	4	722	716
REA1	A	00001138	4	556	
REA10	A	00001378	4	736	
REA11	A	000013B8	4	756	
REA2	A	00001178	4	576	
REA3	A	000011B8	4	596	
REA4	A	000011F8	4	616	
REA5	A	00001238	4	636	
REA6	A	00001278	4	656	
REA7	A	000012B8	4	676	
REA8	A	000012F8	4	696	
REA9	A	00001338	4	716	
READDR	A	00000018	4	450	219
REG2LOW	U	000000DD	1	375	
REG2PATT	U	AABBCCDD	1	374	
RELEN	A	00000014	4	449	
RPTDWSAV	D	000003C0	8	300	289 291
RPTERROR	I	00000398	4	284	256
RPTSAVE	F	000003B8	4	297	284 294
RPTSVR5	F	000003BC	4	298	285 293
SKL0001	U	00000054	1	175	191
SKT0001	C	0000022A	26	172	175 192
SVOLDPSW	U	00000140	0	110	
T1	A	00001120	4	549	775
T10	A	00001360	4	729	784
T11	A	000013A0	4	749	785
T2	A	00001160	4	569	776
T3	A	000011A0	4	589	777
T4	A	000011E0	4	609	778
T5	A	00001220	4	629	779
T6	A	00001260	4	649	780
T7	A	000012A0	4	669	781
T8	A	000012E0	4	689	782
T9	A	00001320	4	709	783
TESTING	F	00001004	4	386	211
TESTREST	U	000002FA	1	218	
TNUM	H	00000004	2	442	210 232
TSUB	A	00000000	4	441	215
TTABLE	F	000013E4	4	774	
V0	U	00000000	1	818	
V1	U	00000001	1	819	213 559 560 579 580 599 600 619 620 639 640 659 660 679 680 699 700 719 720 739 740 759 760
V10	U	0000000A	1	828	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V11	U	0000000B	1	829	
V12	U	0000000C	1	830	
V13	U	0000000D	1	831	
V14	U	0000000E	1	832	
V15	U	0000000F	1	833	
V16	U	00000010	1	834	
V17	U	00000011	1	835	
V18	U	00000012	1	836	
V19	U	00000013	1	837	
V1FUDGE	X	000010D0	16	429	
V1FUDGEB	X	000010E0	16	430	213
V1INPUT	C	000010F0	16	431	
V1OUTPUT	X	000010B0	16	427	220 560 580 600 620 640 660 680 700 720 740 760
V2	U	00000002	1	820	
V20	U	00000014	1	838	
V21	U	00000015	1	839	
V22	U	00000016	1	840	
V23	U	00000017	1	841	
V24	U	00000018	1	842	
V25	U	00000019	1	843	
V26	U	0000001A	1	844	
V27	U	0000001B	1	845	
V28	U	0000001C	1	846	
V29	U	0000001D	1	847	
V3	U	00000003	1	821	
V30	U	0000001E	1	848	
V31	U	0000001F	1	849	
V4	U	00000004	1	822	
V5	U	00000005	1	823	
V6	U	00000006	1	824	
V7	U	00000007	1	825	
V8	U	00000008	1	826	
V9	U	00000009	1	827	
X0001	U	000002B0	1	181	169 182
X1	F	0000113C	4	558	549
X10	F	0000137C	4	738	729
X11	F	000013BC	4	758	749
X2	F	0000117C	4	578	569
X3	F	000011BC	4	598	589
X4	F	000011FC	4	618	609
X5	F	0000123C	4	638	629
X6	F	0000127C	4	658	649
X7	F	000012BC	4	678	669
X8	F	000012FC	4	698	689
X9	F	0000133C	4	718	709
XC0001	U	000002D8	1	195	187
ZVE6TST	J	00000000	5152	107	110 112 116 120 384 108
=A(E6TESTS)	A	000004C0	4	362	201
=AL2(L'MSGMSG)	R	000004CA	2	365	312
=F'1'	F	000004C4	4	363	262
=F'2'	F	000004BC	4	361	186
=H'0'	H	000004C8	2	364	307

```
 MACRO    DEFN  REFERENCES

FCHECK     59   168
PTTABLE   510   773
VRI_H     464   546   566   586   606   626   646   666   686   706   726   746
```

```
   DESC      SYMBOL   SIZE     POS         ADDR

Entry: 0

Image       IMAGE    5152  0000-141F  0000-141F
  Region             5152  0000-141F  0000-141F
    CSECT   ZVE6TST  5152  0000-141F  0000-141F
```

```
   STMT                        FILE NAME
1     /home/tn529/sharedvfp/tests/zvector-e6-10-VLIP.asm

** NO ERRORS FOUND **
```