```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                        2 ************************************************************************
                                                        3 *
                                                        4 *       Zvector E6 instruction tests for VRS-d encoded:
                                                        5 *
                                                        6 *       E63F VECTOR STORE RIGHTMOST WITH LENGTH  (reg)
                                                        7 *
                                                        8 *       also tests
                                                        9 *       E637 VLRLR  - VECTOR LOAD RIGHTMOST WITH LENGTH (reg)
                                                       10 *
                                                       11 *       James Wekel June 2024
                                                       12 ************************************************************************
                                                       13
                                                       14 ************************************************************************
                                                       15 *
                                                       16 *       basic instruction tests
                                                       17 *
                                                       18 ************************************************************************
                                                       19 *  This program tests proper functioning of the z/arch E6 VRS-d vector
                                                       20 *  store rightmost with length (reg). Exceptions are not tested.
                                                       21 *
                                                       22 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                       23 *  obvious coding errors.  None of the tests are thorough.  They are
                                                       24 *  NOT designed to test all aspects of any of the instructions.
                                                       25 *
                                                       26 ************************************************************************
                                                       27 *
                                                       28 *   *Testcase zvector-e6-09-VSTRLR: VECTOR E6 VRS-d VSTRLR instruction
                                                       29 *   *
                                                       30 *   *   Zvector E6 tests for VRS-d encoded instructions:
                                                       31 *   *
                                                       32 *   *   E63F VECTOR STORE RIGHTMOST WITH LENGTH  (reg)
                                                       33 *   *
                                                       34 *   *   # ---------------------------------------------------
                                                       35 *   *   #  This tests only the basic function of the instruction.
                                                       36 *   *   #  Exceptions are NOT tested.
                                                       37 *   *   # ---------------------------------------------------
                                                       38 *   *
                                                       39 *   mainsize    2
                                                       40 *   numcpu      1
                                                       41 *   sysclear
                                                       42 *   archlvl     z/Arch
                                                       43 *
                                                       44 *   diag8cmd    enable    # (needed for messages to Hercules console)
                                                       45 *   loadcore    "$(testpath)/zvector-e6-09-VSTRLR.core" 0x0
                                                       46 *   diag8cmd    disable   # (reset back to default)
                                                       47 *
                                                       48 *   *Done
                                                       49 ************************************************************************
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                      51 ************************************************************************
                                                      52 *        FCHECK Macro - Is a Facility Bit set?
                                                      53 *
                                                      54 *        If the facility bit is NOT set, an message is issued and
                                                      55 *        the test is skipped.
                                                      56 *
                                                      57 *        Fcheck uses R0, R1 and R2
                                                      58 *
                                                      59 * eg.    FCHECK 134,'vector-packed-decimal'
                                                      60 ************************************************************************
                                                      61          MACRO
                                                      62          FCHECK &BITNO,&NOTSETMSG
                                                      63 .*                      &BITNO : facility bit number to check
                                                      64 .*                      &NOTSETMSG : 'facility name'
                                                      65          LCLA  &FBBYTE           Facility bit in Byte
                                                      66          LCLA  &FBBIT            Facility bit within Byte
                                                      67
                                                      68          LCLA  &L(8)
                                                      69 &L(1)    SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                                      70
                                                      71 &FBBYTE  SETA  &BITNO/8
                                                      72 &FBBIT   SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                                      73 .*       MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                                      74
                                                      75          B     X&SYSNDX
                                                      76 *                                       Fcheck data area
                                                      77 *                                       skip messgae
                                                      78 SKT&SYSNDX DC  C'          Skipping tests: '
                                                      79          DC    C&NOTSETMSG
                                                      80          DC    C' facility (bit &BITNO) is not installed.'
                                                      81 SKL&SYSNDX EQU *-SKT&SYSNDX
                                                      82 *                                       facility bits
                                                      83          DS    FD                       gap
                                                      84 FB&SYSNDX DS   4FD
                                                      85          DS    FD                       gap
                                                      86 *
                                                      87 X&SYSNDX EQU *
                                                      88          LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                                      89          STFLE FB&SYSNDX                get facility bits
                                                      90
                                                      91          XGR   R0,R0
                                                      92          IC    R0,FB&SYSNDX+&FBBYTE     get fbit byte
                                                      93          N     R0,=F'&FBBIT'            is bit set?
                                                      94          BNZ   XC&SYSNDX
                                                      95 *
                                                      96 * facility bit not set, issue message and exit
                                                      97 *
                                                      98          LA    R0,SKL&SYSNDX            message length
                                                      99          LA    R1,SKT&SYSNDX            message address
                                                     100          BAL   R2,MSG
                                                     101
                                                     102          B     EOJ
                                                     103 XC&SYSNDX EQU *
                                                     104          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    106 ************************************************************************
                                                    107 *        Low core PSWs
                                                    108 ************************************************************************

                             00000000  000013DF    110 ZVE6TST  START 0
00000000                     00000000                111          USING ZVE6TST,R0            Low core addressability
                                                     112
                             00000140  00000000    113 SVOLDPSW EQU   ZVE6TST+X'140'        z/Arch Supervisor call old PSW

00000000                     00000000  000001A0    115          ORG   ZVE6TST+X'1A0'        z/Architecure RESTART PSW
000001A0  00000001 80000000                         116          DC    X'0000000180000000'
000001A8  00000000 00000200                         117          DC    AD(BEGIN)

000001B0                     000001B0  000001D0    119          ORG   ZVE6TST+X'1D0'        z/Architecure PROGRAM CHECK PSW
000001D0  00020001 80000000                         120          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                         121          DC    AD(X'DEAD')

000001E0                     000001E0  00000200    123          ORG   ZVE6TST+X'200'        Start of actual test program...
                                                    124
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     126 ************************************************************************
                                                     127 *               The actual "ZVE6TST" program itself...
                                                     128 ************************************************************************
                                                     129 *
                                                     130 *  Architecture Mode: z/Arch
                                                     131 *  Register Usage:
                                                     132 *
                                                     133 *   R0       (work)
                                                     134 *   R1-4     (work)
                                                     135 *   R5       Testing control table - current test base
                                                     136 *   R6-R7    (work)
                                                     137 *   R8       First base register
                                                     138 *   R9       Second base register
                                                     139 *   R10      Third base register
                                                     140 *   R11      E6TEST call return
                                                     141 *   R12      E6TESTS register
                                                     142 *   R13      (work)
                                                     143 *   R14      Subroutine call
                                                     144 *   R15      Secondary Subroutine call or work
                                                     145 *
                                                     146 ************************************************************************

00000200                          00000200           148          USING  BEGIN,R8        FIRST Base Register
00000200                          00001200           149          USING  BEGIN+4096,R9   SECOND Base Register
00000200                          00002200           150          USING  BEGIN+8192,R10  THIRD Base Register
                                                     151
00000200  0580                                       152 BEGIN    BALR   R8,0            Initalize FIRST base register
00000202  0680                                       153          BCTR   R8,0            Initalize FIRST base register
00000204  0680                                       154          BCTR   R8,0            Initalize FIRST base register
                                                     155
00000206  4190 8800                      00000800    156          LA     R9,2048(,R8)    Initalize SECOND base register
0000020A  4190 9800                      00000800    157          LA     R9,2048(,R9)    Initalize SECOND base register
                                                     158
0000020E  41A0 9800                      00000800    159          LA     R10,2048(,R9)   Initalize THIRD base register
00000212  41A0 A800                      00000800    160          LA     R10,2048(,R10)  Initalize THIRD base register
                                                     161
00000216  B600 82A4                      000004A4    162          STCTL  R0,R0,CTLR0     Store CR0 to enable AFP
0000021A  9604 82A5                      000004A5    163          OI     CTLR0+1,X'04'   Turn on AFP bit
0000021E  9602 82A5                      000004A5    164          OI     CTLR0+1,X'02'   Turn on Vector bit
00000222  B700 82A4                      000004A4    165          LCTL   R0,R0,CTLR0     Reload updated CR0
                                                     166
                                                     167 ************************************************************************
                                                     168 * Is Vector packed-decimal facility installed  (bit 134)
                                                     169 ************************************************************************
                                                     170
                                                     171          FCHECK 134,'vector-packed-decimal'
00000226  47F0 80B0                      000002B0    172+         B      X0001
                                                     173+*                                  Fcheck data area
                                                     174+*                                  skip messgae
0000022A  40404040 40404040                          175+SKT0001  DC     C'          Skipping tests: '
00000244  A58583A3 96996097                          176+         DC     C'vector-packed-decimal'
00000259  40868183 899389A3                          177+         DC     C' facility (bit 134) is not installed.'
                            00000054  00000001       178+SKL0001  EQU    *-SKT0001
                                                     179+*                                  facility bits
00000280  00000000 00000000                          180+         DS     FD              gap
00000288  00000000 00000000                          181+FB0001   DS     4FD
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
000002A8  00000000 00000000                       182+          DS    FD                        gap
                                                  183+*
                             000002B0  00000001   184+X0001     EQU   *
000002B0  4100 0004                    00000004   185+          LA    R0,((X0001-FB0001)/8)-1
000002B4  B2B0 8088                    00000288   186+          STFLE FB0001                    get facility bits
000002B8  B982 0000                                187+          XGR   R0,R0
000002BC  4300 8098                    00000298   188+          IC    R0,FB0001+16              get fbit byte
000002C0  5400 82AC                    000004AC   189+          N     R0,=F'2'                  is bit set?
000002C4  4770 80D8                    000002D8   190+          BNZ   XC0001
                                                  191+*
                                                  192+* facility bit not set, issue message and exit
                                                  193+*
000002C8  4100 0054                    00000054   194+          LA    R0,SKL0001                message length
000002CC  4110 802A                    0000022A   195+          LA    R1,SKT0001                message address
000002D0  4520 81C0                    000003C0   196+          BAL   R2,MSG
000002D4  47F0 8288                    00000488   197+          B     EOJ
                             000002D8  00000001   198+XC0001    EQU   *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    200 ********************************************************************************
                                                    201 *               Do tests in the E6TESTS table
                                                    202 ********************************************************************************
                                                    203
000002D8  58C0 82B0                       000004B0  204           L     R12,=A(E6TESTS)       get table of test addresses
                                                    205
                                 000002DC  00000001  206 NEXTE6    EQU   *
000002DC  5850 C000                       00000000  207           L     R5,0(0,R12)       get test address
000002E0  1255                                      208           LTR   R5,R5                have a test?
000002E2  4780 8178                       00000378  209           BZ    ENDTEST                 done?
                                                    210
000002E6                          00000000          211           USING E6TEST,R5
                                                    212
000002E6  4800 5004                       00000004  213           LH    R0,TNUM           save current test number
000002EA  5000 8E04                       00001004  214           ST    R0,TESTING        for easy reference
                                                    215
000002EE  E710 8ED0 0006                  000010D0  216           VL    V1,V1FUDGEB       fudge output
000002F4  E710 8EA0 000E                  000010A0  217           VST   v1,V1OUTPUT
000002FA  E710 8EC0 0006                  000010C0  218           VL    V1,V1FUDGE        fudge input
                                                    219
00000300  58B0 5000                       00000000  220           L     R11,TSUB          get address of test routine
00000304  05BB                                      221           BALR  R11,R11           do test
                                                    222
                                 00000306  00000001  223 TESTREST  EQU   *
00000306  E310 501C 0014                  0000001C  224           LGF   R1,READDR         get address of expected result
0000030C  D50F 8EA0 1000          000010A0  00000000  225           CLC   V1OUTPUT,0(R1)    valid?
00000312  4770 811E                       0000031E  226           BNE   FAILMSG                 no, issue failed message
                                                    227
00000316  41C0 C004                       00000004  228           LA    R12,4(0,R12)      next test address
0000031A  47F0 80DC                       000002DC  229           B     NEXTE6
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    231 ************************************************************************
                                                    232 * result not as expected:
                                                    233 *        issue message with test number, instruction under test
                                                    234 *              and instruction l2
                                                    235 ************************************************************************
                               0000031E  00000001   236 FAILMSG  EQU   *
0000031E  4820 5004                      00000004   237          LH    R2,TNUM              get test number and convert
00000322  4E20 8E74                      00001074   238          CVD   R2,DECNUM
00000326  D211 8E5E 8E48       0000105E  00001048   239          MVC   PRT3,EDIT
0000032C  DE11 8E5E 8E74       0000105E  00001074   240          ED    PRT3,DECNUM
00000332  D202 8E18 8E6B       00001018  0000106B   241          MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                    242
00000338  D207 8E33 5010       00001033  00000010   243          MVC   PRTNAME,OPNAME       fill in message with instruction
                                                    244
0000033E  B982 0022                                 245          XGR   R2,R2                get l2 as U32
00000342  5820 5008                      00000008   246          L     R2,L2
00000346  4E20 8E74                      00001074   247          CVD   R2,DECNUM            and convert
0000034A  D211 8E5E 8E48       0000105E  00001048   248          MVC   PRT3,EDIT
00000350  DE11 8E5E 8E74       0000105E  00001074   249          ED    PRT3,DECNUM
00000356  D202 8E44 8E6B       00001044  0000106B   250          MVC   PRTL2(3),PRT3+13     fill in message with l2 field
                                                    251
0000035C  4100 0040                      00000040   252          LA    R0,PRTLNG            message length
00000360  4110 8E08                      00001008   253          LA    R1,PRTLINE           messagfe address
00000364  45F0 8186                      00000386   254          BAL   R15,RPTERROR
```

```
                                                    256 ************************************************************************
                                                    257 * continue after a failed test
                                                    258 ************************************************************************
                               00000368  00000001   259 FAILCONT EQU   *
00000368  5800 82B4                      000004B4   260          L     R0,=F'1'             set GLOBAL failed test indicator
0000036C  5000 8E00                      00001000   261          ST    R0,FAILED
                                                    262
00000370  41C0 C004                      00000004   263          LA    R12,4(0,R12)         next test address
00000374  47F0 80DC                      000002DC   264          B     NEXTE6


                                                    266 ************************************************************************
                                                    267 * end of testing; set ending psw
                                                    268 ************************************************************************
                               00000378  00000001   269 ENDTEST  EQU   *
00000378  5810 8E00                      00001000   270          L     R1,FAILED            did a test fail?
0000037C  1211                                      271          LTR   R1,R1
0000037E  4780 8288                      00000488   272          BZ    EOJ                     No, exit
00000382  47F0 82A0                      000004A0   273          B     FAILTEST                Yes, exit with BAD PSW
                                                    274
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    276 ************************************************************************
                                                    277 *        RPTERROR          Report instruction test in error
                                                    278 *                             R0 = MESSGAE LENGTH
                                                    279 *                             R1 = ADDRESS OF MESSAGE
                                                    280 ************************************************************************

00000386  50F0 81A4                 000003A4    282 RPTERROR ST    R15,RPTSAVE          Save return address
0000038A  5050 81A8                 000003A8    283          ST    R5,RPTSVR5           Save R5
                                                    284 *
                                                    285 *        Use Hercules Diagnose for Message to console
                                                    286 *
0000038E  9002 81B0                 000003B0    287          STM   R0,R2,RPTDWSAV       save regs used by MSG
00000392  4520 81C0                 000003C0    288          BAL   R2,MSG               call Hercules console MSG display
00000396  9802 81B0                 000003B0    289          LM    R0,R2,RPTDWSAV       restore regs


0000039A  5850 81A8                 000003A8    291          L     R5,RPTSVR5           Restore R5
0000039E  58F0 81A4                 000003A4    292          L     R15,RPTSAVE          Restore return address
000003A2  07FF                                  293          BR    R15                  Return to caller

000003A4  00000000                              295 RPTSAVE  DC    F'0'                 R15 save area
000003A8  00000000                              296 RPTSVR5  DC    F'0'                 R5 save area

000003B0  00000000 00000000                     298 RPTDWSAV DC    2D'0'                R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    300 ************************************************************************
                                                    301 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                    302 *              R2 = return address
                                                    303 ************************************************************************
                                                    304
000003C0  4900 82B8                         000004B8  305 MSG      CH    R0,=H'0'                  Do we even HAVE a message?
000003C4  07D2                                        306           BNHR  R2                        No, ignore
                                                    307
000003C6  9002 81FC                         000003FC  308           STM   R0,R2,MSGSAVE             Save registers
                                                    309
000003CA  4900 82BA                         000004BA  310           CH    R0,=AL2(L'MSGMSG)         Message length within limits?
000003CE  47D0 81D6                         000003D6  311           BNH   MSGOK                     Yes, continue
000003D2  4100 005F                         0000005F  312           LA    R0,L'MSGMSG               No, set to maximum
                                                    313
000003D6  1820                                      314 MSGOK     LR    R2,R0                     Copy length to work register
000003D8  0620                                      315           BCTR  R2,0                      Minus-1 for execute
000003DA  4420 8208                         00000408  316           EX    R2,MSGMVC                 Copy message to O/P buffer
                                                    317
000003DE  4120 200A                         0000000A  318           LA    R2,1+L'MSGCMD(,R2)        Calculate true command length
000003E2  4110 820E                         0000040E  319           LA    R1,MSGCMD                 Point to true command
                                                    320
000003E6  83120008                                  321           DC    X'83',X'12',X'0008'       Issue Hercules Diagnose X'008'
000003EA  4780 81F6                         000003F6  322           BZ    MSGRET                    Return if successful
                                                    323
000003EE  1222                                      324           LTR   R2,R2                     Is Diag8 Ry (R2) 0?
000003F0  4780 81F6                         000003F6  325           BZ    MSGRET                      an error occurred but coninue
                                                    326
000003F4  0000                                      327           DC    H'0'                      CRASH for debugging purposes
                                                    328
000003F6  9802 81FC                         000003FC  329 MSGRET   LM    R0,R2,MSGSAVE             Restore registers
000003FA  07F2                                      330           BR    R2                        Return to caller


000003FC  00000000 00000000                         332 MSGSAVE   DC    3F'0'                     Registers save area
00000408  D200 8217 1000      00000417  00000000    333 MSGMVC    MVC   MSGMSG(0),0(R1)           Executed instruction

0000040E  D4E2C7D5 D6C8405C                         335 MSGCMD    DC    C'MSGNOH * '              *** HERCULES MESSAGE COMMAND ***
00000417  40404040 40404040                         336 MSGMSG    DC    CL95' '                   The message text to be displayed
                                                    337
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      339 ************************************************************************
                                                      340 *        Normal completion or Abnormal termination PSWs
                                                      341 ************************************************************************


00000478  00020001 80000000                           343 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)

00000488  B2B2 8278                         00000478  345 EOJ      LPSWE EOJPSW               Normal completion


00000490  00020001 80000000                           347 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')

000004A0  B2B2 8290                         00000490  349 FAILTEST LPSWE FAILPSW              Abnormal termination


                                                      351 ************************************************************************
                                                      352 *        Working Storage
                                                      353 ************************************************************************

000004A4  00000000                                    355 CTLR0    DS    F                    CR0
000004A8  00000000                                    356          DS    F

000004AC                                              358          LTORG ,                    Literals pool
000004AC  00000002                                    359                =F'2'
000004B0  000013B4                                    360                =A(E6TESTS)
000004B4  00000001                                    361                =F'1'
000004B8  0000                                        362                =H'0'
000004BA  005F                                        363                =AL2(L'MSGMSG)
                                                      364
                                                      365 *        some constants
                                                      366
                            00000400  00000001        367 K        EQU   1024                 One KB
                            00001000  00000001        368 PAGE     EQU   (4*K)                Size of one page
                            00010000  00000001        369 K64      EQU   (64*K)               64 KB
                            00100000  00000001        370 MB       EQU   (K*K)                 1 MB
                                                      371
                            AABBCCDD  00000001        372 REG2PATT EQU   X'AABBCCDD'      Polluted Register pattern
                            000000DD  00000001        373 REG2LOW  EQU         X'DD'      (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     375 *=====================================================================
                                                     376 *
                                                     377 *  NOTE: start data on an address that is easy to display
                                                     378 *        within Hercules
                                                     379 *
                                                     380 *=====================================================================
                                                     381
000004BC                      000004BC  00001000     382          ORG   ZVE6TST+X'1000'
00001000  00000000                                   383 FAILED   DC    F'0'                    some test failed?
00001004  00000000                                   384 TESTING  DC    F'0'                    current test number

                                                     386 ************************************************************************
                                                     387 *        TEST failed : result messgae
                                                     388 ************************************************************************
                                                     389 *
                                                     390 *        failed message and associated editting
                                                     391 *
00001008  40404040 40404040                          392 PRTLINE  DC    C'         Test # '
00001018  A7A7A7                                     393 PRTNUM   DC    C'xxx'
0000101B  40868189 93858440                          394          DC    C' failed for instruction '
00001033  A7A7A7A7 A7A7A7A7                          395 PRTNAME  DC    CL8'xxxxxxxx'
0000103B  40A689A3 884093F2                          396          DC    C' with l2='
00001044  A7A7A7                                     397 PRTL2    DC    C'xxx'
00001047  4B                                         398          DC    C'.'
                              00000040  00000001     399 PRTLNG   EQU   *-PRTLINE
                                                     400
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    402 ************************************************************************
                                                    403 *        TEST failed : message working storge
                                                    404 ************************************************************************
00001048  40212020 20202020                        405 EDIT     DC    XL18'4021202020202020202020202020202020'
                                                    406
0000105A  7E7E7E6E                                  407          DC    C'===>'
0000105E  40404040 40404040                        408 PRT3     DC    CL18' '
00001070  4C7E7E7E                                  409          DC    C'<==='
00001074  00000000 00000000                        410 DECNUM   DS    CL16
                                                    411 *
                                                    412 *        CC extrtaction
                                                    413 *
00001084  00000000 00000000                        414 CCPSW    DS    2F          extract PSW after test (has CC)
0000108C  00                                       415 CCFOUND  DS    X           extracted cc


                                                    417 ************************************************************************
                                                    418 *        Vector instruction results, pollution and input
                                                    419 ************************************************************************
00001090                                            420          DS    0FD
00001090  00000000 00000000                        421          DS    XL16                                        gap
000010A0  00000000 00000000                        422 V1OUTPUT DS    XL16                                     V1 OUTPUT
000010B0  00000000 00000000                        423          DS    XL16                                        gap
000010C0  FFFFFFFF FFFFFFFF                        424 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'   V1 FUDGE
000010D0  BBBBBBBB BBBBBBBB                        425 V1FUDGEB DC    XL16'BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB'   V1 FUDGE b
000010E0  F1F2F3F4 F5F6F7F8                        426 V1INPUT  DC    CL16'1234567890123456'                   V1 input
000010F0  F7F8F9F0 F1F2F3F4                        427          DC    CL14'78901234567890'
000010FE  D9                                       428          DC    X'D9'
                                                    429
000010FF  00000000 00000000                        430          DS    XL16                                        gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    432 ************************************************************************
                                                    433 *        E6TEST DSECT
                                                    434 ************************************************************************


                                                    436 E6TEST   DSECT ,
00000000  00000000                                  437 TSUB     DC    A(0)           pointer  to test
00000004  0000                                      438 TNUM     DC    H'00'          Test Number
00000006  00                                        439          DC    X'00'
00000007  00                                        440          DC    X'00'
00000008  00000000                                  441 L2       DC    F'00'          L2 used
0000000C  00000000                                  442 EADDR    DC    A(0)           address of source
                                                    443
00000010  40404040 40404040                        444 OPNAME   DC    CL8' '         E6 name
                                                    445
00000018  00000000                                  446 RELEN    DC    A(0)           RESULT LENGTH
0000001C  00000000                                  447 READDR   DC    A(0)           expected result address
                                                    448
                                                    449 **
                                                    450 *        test routine will be here (from VRS_D macro)
                                                    451 * followed by
                                                    452 *        16-byte EXPECTED RESULT
                                                    453 *        16-byte source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     455 ********************************************************************************
                                                     456 *     Macros to help build test tables
                                                     457 *------------------------------------------------------------------------------
                                                     458 *     VRS_D Macro to help build test tables
                                                     459 ********************************************************************************
                                                     460          MACRO
                                                     461          VRS_D &INST,&L2
                                                     462 .*                                  &INST  - VRS-d instruction under test
                                                     463 .*                                  &L2    - length (loaded into reg)
                                                     464 .*
                                                     465          LCLA  &XCC(4)  &CC has mask values for FAILED condition codes
                                                     466 &XCC(1)  SETA  7                    CC != 0
                                                     467 &XCC(2)  SETA  11                   CC != 1
                                                     468 &XCC(3)  SETA  13                   CC != 2
                                                     469 &XCC(4)  SETA  14                   CC != 3
                                                     470
                                                     471          GBLA  &TNUM
                                                     472 &TNUM    SETA  &TNUM+1
                                                     473
                                                     474          DS    0FD
                                                     475          USING *,R5               base for test data and test routine
                                                     476
                                                     477 T&TNUM   DC    A(X&TNUM)          address of test routine
                                                     478          DC    H'&TNUM'           test number
                                                     479          DC    X'00'
                                                     480          DC    X'00'
                                                     481          DC    F'&L2'             l2
                                                     482 EA2_&TNUM DC   A(RE&TNUM+16)     addr of 16-byte source
                                                     483          DC    CL8'&INST'         instruction name
                                                     484          DC    A(16)              result length
                                                     485 REA&TNUM DC    A(RE&TNUM)         result address
                                                     486 .*
                                                     487 *                                  INSTRUCTION UNDER TEST ROUTINE
                                                     488 X&TNUM   DS    0F
                                                     489          L     R1,L2              get number of bytes to load / store
                                                     490          L     R2,EADDR           get address of source
                                                     491          VLRLR V1,R1,0(R2)        load some bytes
                                                     492
                                                     493          L     R1,L2              get number of bytes to store
                                                     494          &INST V1,R1,V1OUTPUT     test instruction
                                                     495
                                                     496          BR    R11                return
                                                     497
                                                     498 RE&TNUM  DC    0F
                                                     499          DROP  R5
                                                     500
                                                     501          MEND
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                      503 ********************************************************************************
                                                      504 *     PTTABLE Macro to generate table of pointers to individual tests
                                                      505 ********************************************************************************
                                                      506
                                                      507          MACRO
                                                      508          PTTABLE
                                                      509          GBLA  &TNUM
                                                      510          LCLA  &CUR
                                                      511 &CUR     SETA  1
                                                      512 .*
                                                      513 TTABLE   DS    0F
                                                      514 .LOOP    ANOP
                                                      515 .*
                                                      516          DC    A(T&CUR)           address of test
                                                      517 .*
                                                      518 &CUR     SETA  &CUR+1
                                                      519          AIF   (&CUR LE &TNUM).LOOP
                                                      520 *
                                                      521          DC    A(0)               END OF TABLE
                                                      522          DC    A(0)
                                                      523 .*
                                                      524          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     526 ********************************************************************************
                                                     527 *        E6 VRS_D tests
                                                     528 ********************************************************************************
                             00000000  000013DF      529 ZVE6TST  CSECT ,
00001110                                             530          DS    0F


                                                     532          PRINT DATA
                                                     533 *
                                                     534 *        E63F VECTOR STORE RIGHTMOST WITH LENGTH  (reg)
                                                     535 *
                                                     536 *        VRS_D instr,l2
                                                     537 *              followed by
                                                     538 *              v1     - 16 byte expected result
                                                     539 *              source - 16 byte source from which to get
                                                     540 *                       L2+1 (up to 16) bytes
                                                     541
                                                     542 *-------------------------------------------------------------------
                                                     543 *VSTRLR  - VECTOR STORE RIGHTMOST WITH LENGTH  (reg)
                                                     544 *-------------------------------------------------------------------
                                                     545 * VSTRLR simple
                                                     546
                                                     547          VRS_D VSTRLR,0                                  1-byte
00001110                                             548+         DS    0FD
00001110                             00001110        549+         USING *,R5              base for test data and test routine
00001110  00001130                                   550+T1       DC    A(X1)             address of test routine
00001114  0001                                       551+         DC    H'1'              test number
00001116  00                                         552+         DC    X'00'
00001117  00                                         553+         DC    X'00'
00001118  00000000                                   554+         DC    F'0'              l2
0000111C  0000115C                                   555+EA2_1    DC    A(RE1+16)        addr of 16-byte source
00001120  E5E2E3D9 D3D94040                          556+         DC    CL8'VSTRLR'       instruction name
00001128  00000010                                   557+         DC    A(16)             result length
0000112C  0000114C                                   558+REA1     DC    A(RE1)            result address
                                                     559+*                                  INSTRUCTION UNDER TEST ROUTINE
00001130                                             560+X1       DS    0F
00001130  5810 5008                      00000008    561+         L     R1,L2             get number of bytes to load / store
00001134  5820 500C                      0000000C    562+         L     R2,EADDR          get address of source
00001138  E601 2000 1037                 00000000    563+         VLRLR V1,R1,0(R2)       load some bytes
0000113E  5810 5008                      00000008    564+         L     R1,L2             get number of bytes to store
00001142  E601 8EA0 103F                 000010A0    565+         VSTRLR V1,R1,V1OUTPUT   test instruction
00001148  07FB                                       566+         BR    R11               return
0000114C                                             567+RE1      DC    0F
0000114C                                             568+         DROP  R5
0000114C  22BBBBBB BBBBBBBB                          569          DC    XL16'22BBBBBBBBBBBBBBBBBBBBBBBBBBBBBB'   V1
00001154  BBBBBBBB BBBBBBBB
0000115C  22000000 00000000                          570          DC    XL16'2200000000000000000000000000023C'   source
00001164  00000000 0000023C
                                                     571
                                                     572          VRS_D VSTRLR,1
00001170                                             573+         DS    0FD
00001170                             00001170        574+         USING *,R5              base for test data and test routine
00001170  00001190                                   575+T2       DC    A(X2)             address of test routine
00001174  0002                                       576+         DC    H'2'              test number
00001176  00                                         577+         DC    X'00'
00001177  00                                         578+         DC    X'00'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001178  00000001                                579+          DC    F'1'               l2
0000117C  000011BC                                580+EA2_2     DC    A(RE2+16)         addr of 16-byte source
00001180  E5E2E3D9 D3D94040                       581+          DC    CL8'VSTRLR'        instruction name
00001188  00000010                                582+          DC    A(16)              result length
0000118C  000011AC                                583+REA2      DC    A(RE2)             result address
                                                  584+*                                  INSTRUCTION UNDER TEST ROUTINE
00001190                                          585+X2        DS    0F
00001190  5810 5008                     00000008  586+          L     R1,L2              get number of bytes to load / store
00001194  5820 500C                     0000000C  587+          L     R2,EADDR           get address of source
00001198  E601 2000 1037                00000000  588+          VLRLR V1,R1,0(R2)        load some bytes
0000119E  5810 5008                     00000008  589+          L     R1,L2              get number of bytes to store
000011A2  E601 8EA0 103F                000010A0  590+          VSTRLR V1,R1,V1OUTPUT    test instruction
000011A8  07FB                                    591+          BR    R11                return
000011AC                                          592+RE2       DC    0F
000011AC                                          593+          DROP  R5
000011AC  2233BBBB BBBBBBBB                       594           DC    XL16'2233BBBBBBBBBBBBBBBBBBBBBBBB'    V1
000011B4  BBBBBBBB BBBBBBBB
000011BC  22330000 00000000                       595           DC    XL16'2233000000000000000000000000023C'   source
000011C4  00000000 0000023C
                                                  596
                                                  597           VRS_D VSTRLR,5
000011D0                                          598+          DS    0FD
000011D0                  000011D0                599+          USING *,R5               base for test data and test routine
000011D0  000011F0                                600+T3        DC    A(X3)              address of test routine
000011D4  0003                                    601+          DC    H'3'               test number
000011D6  00                                      602+          DC    X'00'
000011D7  00                                      603+          DC    X'00'
000011D8  00000005                                604+          DC    F'5'               l2
000011DC  0000121C                                605+EA2_3     DC    A(RE3+16)         addr of 16-byte source
000011E0  E5E2E3D9 D3D94040                       606+          DC    CL8'VSTRLR'        instruction name
000011E8  00000010                                607+          DC    A(16)              result length
000011EC  0000120C                                608+REA3      DC    A(RE3)             result address
                                                  609+*                                  INSTRUCTION UNDER TEST ROUTINE
000011F0                                          610+X3        DS    0F
000011F0  5810 5008                     00000008  611+          L     R1,L2              get number of bytes to load / store
000011F4  5820 500C                     0000000C  612+          L     R2,EADDR           get address of source
000011F8  E601 2000 1037                00000000  613+          VLRLR V1,R1,0(R2)        load some bytes
000011FE  5810 5008                     00000008  614+          L     R1,L2              get number of bytes to store
00001202  E601 8EA0 103F                000010A0  615+          VSTRLR V1,R1,V1OUTPUT    test instruction
00001208  07FB                                    616+          BR    R11                return
0000120C                                          617+RE3       DC    0F
0000120C                                          618+          DROP  R5
0000120C  22334455 6677BBBB                       619           DC    XL16'223344556677BBBBBBBBBBBBBBBBBBBB'    V1
00001214  BBBBBBBB BBBBBBBB
0000121C  22334455 66778800                       620           DC    XL16'2233445566778800000000000000023C'   source
00001224  00000000 0000023C
                                                  621
                                                  622           VRS_D VSTRLR,14
00001230                                          623+          DS    0FD
00001230                  00001230                624+          USING *,R5               base for test data and test routine
00001230  00001250                                625+T4        DC    A(X4)              address of test routine
00001234  0004                                    626+          DC    H'4'               test number
00001236  00                                      627+          DC    X'00'
00001237  00                                      628+          DC    X'00'
00001238  0000000E                                629+          DC    F'14'              l2
0000123C  0000127C                                630+EA2_4     DC    A(RE4+16)         addr of 16-byte source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001240  E5E2E3D9 D3D94040                          631+          DC    CL8'VSTRLR'       instruction name
00001248  00000010                                   632+          DC    A(16)             result length
0000124C  0000126C                                   633+REA4      DC    A(RE4)            result address
                                                     634+*                                 INSTRUCTION UNDER TEST ROUTINE
00001250                                             635+X4        DS    0F
00001250  5810 5008                        00000008  636+          L     R1,L2             get number of bytes to load / store
00001254  5820 500C                        0000000C  637+          L     R2,EADDR          get address of source
00001258  E601 2000 1037                   00000000  638+          VLRLR V1,R1,0(R2)       load some bytes
0000125E  5810 5008                        00000008  639+          L     R1,L2             get number of bytes to store
00001262  E601 8EA0 103F                   000010A0  640+          VSTRLR V1,R1,V1OUTPUT   test instruction
00001268  07FB                                       641+          BR    R11               return
0000126C                                             642+RE4       DC    0F
0000126C                                             643+          DROP  R5
0000126C  22334455 66778800                          644           DC    XL16'223344556677880000000000000002BB'    V1
00001274  00000000 000002BB
0000127C  22334455 66778800                          645           DC    XL16'223344556677880000000000000023C'   source
00001284  00000000 0000023C
                                                     646
                                                     647           VRS_D VSTRLR,15
00001290                                             648+          DS    0FD
00001290                   00001290                  649+          USING *,R5              base for test data and test routine
00001290  000012B0                                   650+T5        DC    A(X5)             address of test routine
00001294  0005                                       651+          DC    H'5'              test number
00001296  00                                         652+          DC    X'00'
00001297  00                                         653+          DC    X'00'
00001298  0000000F                                   654+          DC    F'15'             l2
0000129C  000012DC                                   655+EA2_5     DC    A(RE5+16)       addr of 16-byte source
000012A0  E5E2E3D9 D3D94040                          656+          DC    CL8'VSTRLR'        instruction name
000012A8  00000010                                   657+          DC    A(16)              result length
000012AC  000012CC                                   658+REA5      DC    A(RE5)             result address
                                                     659+*                                 INSTRUCTION UNDER TEST ROUTINE
000012B0                                             660+X5        DS    0F
000012B0  5810 5008                        00000008  661+          L     R1,L2             get number of bytes to load / store
000012B4  5820 500C                        0000000C  662+          L     R2,EADDR          get address of source
000012B8  E601 2000 1037                   00000000  663+          VLRLR V1,R1,0(R2)       load some bytes
000012BE  5810 5008                        00000008  664+          L     R1,L2             get number of bytes to store
000012C2  E601 8EA0 103F                   000010A0  665+          VSTRLR V1,R1,V1OUTPUT   test instruction
000012C8  07FB                                       666+          BR    R11               return
000012CC                                             667+RE5       DC    0F
000012CC                                             668+          DROP  R5
000012CC  22334455 66778800                          669           DC    XL16'223344556677880000000000000023C'    V1
000012D4  00000000 0000023C
000012DC  22334455 66778800                          670           DC    XL16'223344556677880000000000000023C'   source
000012E4  00000000 0000023C
                                                     671
                                                     672           VRS_D VSTRLR,32                      check r3>15
000012F0                                             673+          DS    0FD
000012F0                   000012F0                  674+          USING *,R5              base for test data and test routine
000012F0  00001310                                   675+T6        DC    A(X6)             address of test routine
000012F4  0006                                       676+          DC    H'6'              test number
000012F6  00                                         677+          DC    X'00'
000012F7  00                                         678+          DC    X'00'
000012F8  00000020                                   679+          DC    F'32'             l2
000012FC  0000133C                                   680+EA2_6     DC    A(RE6+16)       addr of 16-byte source
00001300  E5E2E3D9 D3D94040                          681+          DC    CL8'VSTRLR'        instruction name
00001308  00000010                                   682+          DC    A(16)              result length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
0000130C  0000132C                                683+REA6     DC    A(RE6)            result address
                                                  684+*                                INSTRUCTION UNDER TEST ROUTINE
00001310                                          685+X6       DS    0F
00001310  5810 5008                   00000008    686+         L     R1,L2             get number of bytes to load / store
00001314  5820 500C                   0000000C    687+         L     R2,EADDR          get address of source
00001318  E601 2000 1037              00000000    688+         VLRLR V1,R1,0(R2)       load some bytes
0000131E  5810 5008                   00000008    689+         L     R1,L2             get number of bytes to store
00001322  E601 8EA0 103F              000010A0    690+         VSTRLR V1,R1,V1OUTPUT   test instruction
00001328  07FB                                    691+         BR    R11               return
0000132C                                          692+RE6      DC    0F
0000132C                                          693+         DROP  R5
0000132C  22334455 66778800                       694          DC    XL16'223344556677880000000000000023C'    V1
00001334  00000000 0000023C
0000133C  22334455 66778800                       695          DC    XL16'223344556677880000000000000023C'   source
00001344  00000000 0000023C
                                                  696
                                                  697          VRS_D VSTRLR,999                      check r3>15
00001350                                          698+         DS    0FD
00001350                      00001350            699+         USING *,R5              base for test data and test routine
00001350  00001370                                700+T7       DC    A(X7)             address of test routine
00001354  0007                                    701+         DC    H'7'              test number
00001356  00                                      702+         DC    X'00'
00001357  00                                      703+         DC    X'00'
00001358  000003E7                                704+         DC    F'999'            l2
0000135C  0000139C                                705+EA2_7    DC    A(RE7+16)        addr of 16-byte source
00001360  E5E2E3D9 D3D94040                       706+         DC    CL8'VSTRLR'       instruction name
00001368  00000010                                707+         DC    A(16)             result length
0000136C  0000138C                                708+REA7     DC    A(RE7)            result address
                                                  709+*                                INSTRUCTION UNDER TEST ROUTINE
00001370                                          710+X7       DS    0F
00001370  5810 5008                   00000008    711+         L     R1,L2             get number of bytes to load / store
00001374  5820 500C                   0000000C    712+         L     R2,EADDR          get address of source
00001378  E601 2000 1037              00000000    713+         VLRLR V1,R1,0(R2)       load some bytes
0000137E  5810 5008                   00000008    714+         L     R1,L2             get number of bytes to store
00001382  E601 8EA0 103F              000010A0    715+         VSTRLR V1,R1,V1OUTPUT   test instruction
00001388  07FB                                    716+         BR    R11               return
0000138C                                          717+RE7      DC    0F
0000138C                                          718+         DROP  R5
0000138C  99334455 66778800                       719          DC    XL16'993344556677880000000000009023C'    V1
00001394  00000000 0009023C
0000139C  99334455 66778800                       720          DC    XL16'993344556677880000000000009023C'   source
000013A4  00000000 0009023C
                                                  721
000013AC  00000000                                722          DC    F'0'     END OF TABLE
000013B0  00000000                                723          DC    F'0'
                                                  724 *
                                                  725 * table of pointers to individual load test
                                                  726 *
000013B4                                          727 E6TESTS  DS    0F
                                                  728          PTTABLE
000013B4                                          729+TTABLE   DS    0F
000013B4  00001110                                730+         DC    A(T1)             address of test
000013B8  00001170                                731+         DC    A(T2)             address of test
000013BC  000011D0                                732+         DC    A(T3)             address of test
000013C0  00001230                                733+         DC    A(T4)             address of test
000013C4  00001290                                734+         DC    A(T5)             address of test
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

000013C8  000012F0                            735+          DC    A(T6)             address of test
000013CC  00001350                            736+          DC    A(T7)             address of test
                                              737+*
000013D0  00000000                            738+          DC    A(0)              END OF TABLE
000013D4  00000000                            739+          DC    A(0)
                                              740
000013D8  00000000                            741           DC    F'0'     END OF TABLE
000013DC  00000000                            742           DC    F'0'
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   744 ********************************************************************************
                                                   745 *        Register equates
                                                   746 ********************************************************************************

                                00000000  00000001   748 R0       EQU   0
                                00000001  00000001   749 R1       EQU   1
                                00000002  00000001   750 R2       EQU   2
                                00000003  00000001   751 R3       EQU   3
                                00000004  00000001   752 R4       EQU   4
                                00000005  00000001   753 R5       EQU   5
                                00000006  00000001   754 R6       EQU   6
                                00000007  00000001   755 R7       EQU   7
                                00000008  00000001   756 R8       EQU   8
                                00000009  00000001   757 R9       EQU   9
                                0000000A  00000001   758 R10      EQU   10
                                0000000B  00000001   759 R11      EQU   11
                                0000000C  00000001   760 R12      EQU   12
                                0000000D  00000001   761 R13      EQU   13
                                0000000E  00000001   762 R14      EQU   14
                                0000000F  00000001   763 R15      EQU   15
```

```
                                                   765 ********************************************************************************
                                                   766 *        Register equates
                                                   767 ********************************************************************************

                                00000000  00000001   769 V0       EQU   0
                                00000001  00000001   770 V1       EQU   1
                                00000002  00000001   771 V2       EQU   2
                                00000003  00000001   772 V3       EQU   3
                                00000004  00000001   773 V4       EQU   4
                                00000005  00000001   774 V5       EQU   5
                                00000006  00000001   775 V6       EQU   6
                                00000007  00000001   776 V7       EQU   7
                                00000008  00000001   777 V8       EQU   8
                                00000009  00000001   778 V9       EQU   9
                                0000000A  00000001   779 V10      EQU   10
                                0000000B  00000001   780 V11      EQU   11
                                0000000C  00000001   781 V12      EQU   12
                                0000000D  00000001   782 V13      EQU   13
                                0000000E  00000001   783 V14      EQU   14
                                0000000F  00000001   784 V15      EQU   15
                                00000010  00000001   785 V16      EQU   16
                                00000011  00000001   786 V17      EQU   17
                                00000012  00000001   787 V18      EQU   18
                                00000013  00000001   788 V19      EQU   19
                                00000014  00000001   789 V20      EQU   20
                                00000015  00000001   790 V21      EQU   21
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                00000016  00000001   791 V22      EQU   22
                                00000017  00000001   792 V23      EQU   23
                                00000018  00000001   793 V24      EQU   24
                                00000019  00000001   794 V25      EQU   25
                                0000001A  00000001   795 V26      EQU   26
                                0000001B  00000001   796 V27      EQU   27
                                0000001C  00000001   797 V28      EQU   28
                                0000001D  00000001   798 V29      EQU   29
                                0000001E  00000001   799 V30      EQU   30
                                0000001F  00000001   800 V31      EQU   31
                                                     801
                                                     802          END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
BEGIN	I	00000200	2	152	117 148 149 150
CCFOUND	X	0000108C	1	415	
CCPSW	F	00001084	4	414	
CTLR0	F	000004A4	4	355	162 163 164 165
DECNUM	C	00001074	16	410	238 240 247 249
E6TEST	4	00000000	32	436	211
E6TESTS	F	000013B4	4	727	204
EA2_1	A	0000111C	4	555	
EA2_2	A	0000117C	4	580	
EA2_3	A	000011DC	4	605	
EA2_4	A	0000123C	4	630	
EA2_5	A	0000129C	4	655	
EA2_6	A	000012FC	4	680	
EA2_7	A	0000135C	4	705	
EADDR	A	0000000C	4	442	562 587 612 637 662 687 712
EDIT	X	00001048	18	405	239 248
ENDTEST	U	00000378	1	269	209
EOJ	I	00000488	4	345	197 272
EOJPSW	D	00000478	8	343	345
FAILCONT	U	00000368	1	259	
FAILED	F	00001000	4	383	261 270
FAILMSG	U	0000031E	1	236	226
FAILPSW	D	00000490	8	347	349
FAILTEST	I	000004A0	4	349	273
FB0001	F	00000288	8	181	185 186 188
IMAGE	1	00000000	5088	0	
K	U	00000400	1	367	368 369 370
K64	U	00010000	1	369	
L2	F	00000008	4	441	246 561 564 586 589 611 614 636 639 661 664 686 689 711 714
MB	U	00100000	1	370	
MSG	I	000003C0	4	305	196 288
MSGCMD	C	0000040E	9	335	318 319
MSGMSG	C	00000417	95	336	312 333 310
MSGMVC	I	00000408	6	333	316
MSGOK	I	000003D6	2	314	311
MSGRET	I	000003F6	4	329	322 325
MSGSAVE	F	000003FC	4	332	308 329
NEXTE6	U	000002DC	1	206	229 264
OPNAME	C	00000010	8	444	243
PAGE	U	00001000	1	368	
PRT3	C	0000105E	18	408	239 240 241 248 249 250
PRTL2	C	00001044	3	397	250
PRTLINE	C	00001008	16	392	399 253
PRTLNG	U	00000040	1	399	252
PRTNAME	C	00001033	8	395	243
PRTNUM	C	00001018	3	393	241
R0	U	00000000	1	748	111 162 165 185 187 188 189 194 213 214 252 260 261 287 289 305 308 310 312 314 329
R1	U	00000001	1	749	195 224 225 253 270 271 319 333 561 563 564 565 586 588 589 590 611 613 614 615 636 638 639 640 661 663 664 665 686 688 689 690 711 713 714 715
R10	U	0000000A	1	758	150 159 160
R11	U	0000000B	1	759	220 221 566 591 616 641 666 691 716
R12	U	0000000C	1	760	204 207 228 263
R13	U	0000000D	1	761	
R14	U	0000000E	1	762	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
R15	U	0000000F	1	763	254 282 292 293
R2	U	00000002	1	750	196 237 238 245 246 247 287 288 289 306 308 314 315 316 318 324 329 330 562 563 587 588 612 613 637 638 662 663 687 688 712 713
R3	U	00000003	1	751	
R4	U	00000004	1	752	
R5	U	00000005	1	753	207 208 211 283 291 549 568 574 593 599 618 624 643 649 668 674 693 699 718
R6	U	00000006	1	754	
R7	U	00000007	1	755	
R8	U	00000008	1	756	148 152 153 154 156
R9	U	00000009	1	757	149 156 157 159
RE1	F	0000114C	4	567	555 558
RE2	F	000011AC	4	592	580 583
RE3	F	0000120C	4	617	605 608
RE4	F	0000126C	4	642	630 633
RE5	F	000012CC	4	667	655 658
RE6	F	0000132C	4	692	680 683
RE7	F	0000138C	4	717	705 708
REA1	A	0000112C	4	558	
REA2	A	0000118C	4	583	
REA3	A	000011EC	4	608	
REA4	A	0000124C	4	633	
REA5	A	000012AC	4	658	
REA6	A	0000130C	4	683	
REA7	A	0000136C	4	708	
READDR	A	0000001C	4	447	224
REG2LOW	U	000000DD	1	373	
REG2PATT	U	AABBCCDD	1	372	
RELEN	A	00000018	4	446	
RPTDWSAV	D	000003B0	8	298	287 289
RPTERROR	I	00000386	4	282	254
RPTSAVE	F	000003A4	4	295	282 292
RPTSVR5	F	000003A8	4	296	283 291
SKL0001	U	00000054	1	178	194
SKT0001	C	0000022A	26	175	178 195
SVOLDPSW	U	00000140	0	113	
T1	A	00001110	4	550	730
T2	A	00001170	4	575	731
T3	A	000011D0	4	600	732
T4	A	00001230	4	625	733
T5	A	00001290	4	650	734
T6	A	000012F0	4	675	735
T7	A	00001350	4	700	736
TESTING	F	00001004	4	384	214
TESTREST	U	00000306	1	223	
TNUM	H	00000004	2	438	213 237
TSUB	A	00000000	4	437	220
TTABLE	F	000013B4	4	729	
V0	U	00000000	1	769	
V1	U	00000001	1	770	216 217 218 563 565 588 590 613 615 638 640 663 665 688 690 713 715
V10	U	0000000A	1	779	
V11	U	0000000B	1	780	
V12	U	0000000C	1	781	
V13	U	0000000D	1	782	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V14	U	0000000E	1	783	
V15	U	0000000F	1	784	
V16	U	00000010	1	785	
V17	U	00000011	1	786	
V18	U	00000012	1	787	
V19	U	00000013	1	788	
V1FUDGE	X	000010C0	16	424	218
V1FUDGEB	X	000010D0	16	425	216
V1INPUT	C	000010E0	16	426	
V1OUTPUT	X	000010A0	16	422	217 225 565 590 615 640 665 690 715
V2	U	00000002	1	771	
V20	U	00000014	1	789	
V21	U	00000015	1	790	
V22	U	00000016	1	791	
V23	U	00000017	1	792	
V24	U	00000018	1	793	
V25	U	00000019	1	794	
V26	U	0000001A	1	795	
V27	U	0000001B	1	796	
V28	U	0000001C	1	797	
V29	U	0000001D	1	798	
V3	U	00000003	1	772	
V30	U	0000001E	1	799	
V31	U	0000001F	1	800	
V4	U	00000004	1	773	
V5	U	00000005	1	774	
V6	U	00000006	1	775	
V7	U	00000007	1	776	
V8	U	00000008	1	777	
V9	U	00000009	1	778	
X0001	U	000002B0	1	184	172 185
X1	F	00001130	4	560	550
X2	F	00001190	4	585	575
X3	F	000011F0	4	610	600
X4	F	00001250	4	635	625
X5	F	000012B0	4	660	650
X6	F	00001310	4	685	675
X7	F	00001370	4	710	700
XC0001	U	000002D8	1	198	190
ZVE6TST	J	00000000	5088	110	113 115 119 123 382 111
=A(E6TESTS)	A	000004B0	4	360	204
=AL2(L'MSGMSG)	R	000004BA	2	363	310
=F'1'	F	000004B4	4	361	260
=F'2'	F	000004AC	4	359	189
=H'0'	H	000004B8	2	362	305

```
 MACRO   DEFN  REFERENCES

FCHECK    62   171
PTTABLE  508   728
VRS_D    461   547   572   597   622   647   672   697
```

```
   DESC      SYMBOL   SIZE     POS         ADDR

Entry: 0

Image       IMAGE    5088  0000-13DF  0000-13DF
  Region             5088  0000-13DF  0000-13DF
    CSECT   ZVE6TST  5088  0000-13DF  0000-13DF
```

```
   STMT                         FILE NAME
1     /home/tn529/sharedvfp/tests/zvector-e6-09-VSTRLR.asm

** NO ERRORS FOUND **
```